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MECL

SYSTEM DESIGN HANDBOOK

NEW REVISED EDITION

MOTOROLA Semiconductor Products Inc.

MECL

SYSTEM DESIGN HANDBOOK

Second Edition

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MOTOROLA *Semiconductor Products Inc.*

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PREFACE

In response to the demand for higher performance systems, engineers are looking at digital integrated circuit families which are faster than the popular TTL and DTL types. Motorola's Emitter Coupled Logic (MECL) circuits have the characteristics to meet the performance requirements for present and future systems. MECL 10,000 is ideal for computer and communications systems, while state-of-the-art instrumentation equipment uses MECL III.

As circuit speeds increase, wiring rules and system design techniques must be adjusted accordingly. Designing with MECL is no more difficult than designing high performance equipment with slower forms of logic. High performance system design for any form of logic, however, does require an understanding of the factors which affect system performance. In fact, many of the MECL features such as transmission line drive capability, complementary outputs, Wired-OR, and versatile logic functions can add as much to system performance as the short propagation delays and high toggle rates.

In the past, several articles and application notes have been written about MECL circuits and systems. However, there was a need for a book which would completely define MECL operation. This book has been written to give the designer the information to establish design rules for his own high performance systems.

The information in this book is based on equations derived from electronic theory, laboratory tests, and inputs from MECL users. All of the rules and tables are for conservative system design with MECL circuits. It is important to realize that the circuits can operate properly under conditions much more adverse than suggested in this book.

In addition to the technical contributors, Jon DeLaune and Jerry Prioste, the author would like to thank Lloyd Maul, Mike Lee, Reg Hamer, Jim Hively, Howard Gnauden, Don Murray, Tom Balph, and Colin Crook whose knowledge of MECL has added to the completeness and accuracy of this book. Finally, great appreciation is due to the many technicians, engineers, and managers who took their valuable time to read all or part of this book as it was developed.

This edition differs from the first primarily because of the addition of chapters 9 and 10, and a brief appendix describing some of the hardware and components available for MECL Systems. The few minor errors discovered in the first edition have also been corrected. The author wishes to thank George Adams for preparing Chapter 10 in this edition.

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Introduction

What is MECL?

The term MECL identifies Motorola's emitter coupled logic. Emitter coupled logic is a non-saturating form of digital logic which eliminates transistor storage time as a speed limiting characteristic, permitting very high speed operation. "Emitter Coupled" refers to the manner in which the emitters of a differential amplifier within the integrated circuit are connected. The differential amplifier provides high impedance inputs and voltage gain within the circuit. Emitter follower outputs restore the logic levels and provide low output impedance for good line driving and high fanout capability.

History of MECL

Motorola offers MECL circuits in four logic families: MECL I, MECL II, MECL III, and MECL 10,000.

The MECL I family was the first digital monolithic integrated circuit line produced by Motorola. Introduced in 1962, MECL I was considerably beyond the state-of-the-art at that time. Several years passed before any other form of logic could equal the 8 ns gate propagation delays and 30 MHz toggle rates of MECL I. As a result of its reliability and performance, MECL I was designed into many advanced systems.

Nearly a decade later, MECL I is still being produced by Motorola. It finds wide usage in existing products. However, several features of the more advanced MECL II, III, and 10,000 favor their being used in new designs. For example, MECL I requires a separate bias driver package, MC304/MC354, to be connected to the logic functions. This means increased package count and extra circuit board wiring. Also the 10-pin packages used for MECL I limit the number of gates per package and the number of gate inputs. No provision was made for operation of MECL I with transmission lines, as they were unnecessary with the 8 ns rise and fall times.

In 1966 Motorola introduced the more advanced MECL II. The basic gate featured 4 ns propagation delays and flip-flop circuits that would toggle at over 70 MHz. MECL II immediately set a new standard for performance that has been equaled by non-ECL logic only with the introduction of Schottky TTL in 1970.

Motorola continued with the development of MECL II and flip-flop speeds were increased first to 120 MHz for the MC1027/MC1227 JK circuit, and then to 180 MHz for the MC1034 type D flip-flop. To drive these high speed flip-flops, high speed line drivers were introduced with 2 ns propagation delays and 2 ns rise and fall times. With 2 ns edges, transmission lines could be used to preserve the waveforms and limit overshoot and ringing on longer lines. Consequently, the MC1026 was designed to drive 50-ohm lines. Because of the significant speed increase of the line drivers and high speed flip-flops over the basic MECL II parts, these circuits are commonly called MECL II-1/2, although they are part of the MECL II family.

MECL II is continuing to gain in popularity and is being designed into many high speed systems. MECL II circuits have a temperature compensated bias driver internal to the circuits (except for the MC1020/MC1220 line receiver which requires no internal bias). The internal bias source simplifies circuit interconnections and tracks with both temperature and supply voltage to retain noise margin under varied operating conditions.

Complex functions became available in MECL II when trends shifted toward more complicated circuits. The family now has adders, data selectors, multiplexers, decoders and a Nixie* tube decoder/driver. MECL II is a growing line, with new products currently being designed and introduced.

Motorola's continuing development of ECL made possible an even faster logic family. As a result, MECL III was introduced in 1968. Its 1 ns gate propagation delays and greater than 500 MHz flip-flop toggle rates remain the industry leaders. The 1 ns rise and fall times require a transmission line environment for all but the smallest systems. For this reason, all circuit outputs are designed to drive transmission lines and all output logic levels are specified when driving 50-ohm loads. Because of MECL III's fast edge speeds, multi-layer boards are recommended above 200 MHz. For the first time with MECL, internal input pulldown resistors are included with the circuits to eliminate the need to tie unused inputs to V_{EE}. The Hi-Z 50 kΩ input resistors are used with transmission lines for most applications. Optional Low-Z 2 kΩ input resistors can be used in place of pulldown resistors when the chips are used in a hybrid circuit or when line lengths are very short. MECL III is gaining in popularity – especially in high speed test and communications equipment. As a result, Motorola is continuing to expand and develop this product line.

Trends in large high speed systems have shown the need for an easy to use logic family with 2 ns propagation delays. To fill this requirement, Motorola introduced the MECL 10,000 series in 1971. In order to make the circuits comparatively easy to use, edge speed was slowed to 3.5 ns while the important propagation delay was held to 2.0 ns. The slow edge speed permits use of wire wrap and standard printed circuit lines. However, the circuits are specified to drive transmission lines for optimum performance.

MECL 10,000 is provided with logic levels that are completely compatible with MECL III to facilitate using both families in the same system. A second important feature of MECL 10,000 is the significant power reduction. MECL 10,000 gates use less than one-half the power of MECL III or high speed MECL II gates. Finally, the low gate power and advanced circuit design techniques have permitted a new level of MECL complex circuits. For example, complexity of the MC10181 four-bit arithmetic unit compares favorably to that of any bipolar integrated circuit on the market. MECL 10,000 is the fastest growing ECL family in the industry and Motorola is designing and introducing many versatile complex functions to expand the line.

Why Use MECL?

Circuit speed is, of course, an obvious reason for designing with MECL. MECL III is significantly faster than any other digital logic family. MECL 10,000 offers shorter propagation delays and higher toggle rates than any non-ECL type of

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*T.M. – Burroughs Corp.

logic. Equally important to the circuit speed are the characteristics of MECL circuits which permit entire systems to operate at high speeds.

The ability of the faster MECL families to drive transmission lines becomes increasingly important in larger and faster systems. While a transmission line environment imposes some additional design rules and restrictions, the advantages of longer signal paths, better fanout, improved noise immunity, and faster operation, often more than compensate for the restrictions.

When using MECL II or MECL 10,000 without transmission lines, their high input impedances permit the use of series-damping resistors to increase wiring lengths and to improve waveforms. Unlike non-ECL forms of logic, MECL circuits have constant power supply requirements, independent of operating frequency. This simplifies power supply design, since circuit speed need not be considered a variable. At fast circuit speeds MECL can offer a considerable power saving over the other types of logic.

In addition to faster operation, the line driving features of MECL circuits can be exploited to improve system performance. For one, the parts specified to drive transmission lines will drive coaxial cables over distances limited only by the bandwidth of the cable. In addition, the shielding in coaxial cable gives good isolation from external noise.

More economical than using coaxial cable, is the ability of the MECL circuits to differentially drive and receive signals on twisted pair lines. Using this technique, signals have been sent over twisted pair lines up to 1000 feet in length.

The complementary outputs and Wired-OR capabilities of MECL circuits result in faster system operation with reduced package count and a power saving. The complementary outputs are inherent in the circuit design and both outputs have equal propagation delay. This eliminates the timing problems associated with using an inverter to get a complement signal. The logic OR function is obtained by wiring circuit-outputs together. The propagation delay of the Wired-OR connection is much less than a gate function and can save power, as only one pulldown resistor or termination is required per Wired-OR.

Another advantage when designing with MECL is the low noise generated by the circuits. Unlike totem pole outputs, the emitter follower does not generate a large current spike when switching logic states, so the power lines stay comparatively noise free. The low current-switching in signal paths, relatively small voltage swing (typically 800 mV), and low output impedances, cut down crosstalk and noise.

Generated noise is also reduced by MECL's relatively slow rise and fall times. For each MECL family the edge speed is equal to or greater than the propagation delay. The low noise associated with MECL is especially important when the logic circuits are to be used in a system which contains low level analog or communications signals.

The flexibility of the MECL line receivers and Schmitt triggers to act as linear amplifiers leads to many functions that may be performed with standard MECL circuits. For example, in addition to amplifying low level signals to MECL levels, these MECL circuits can be used as crystal oscillators, zero crossing detectors, power buffers, Schmitt triggers, RF and video amplifiers, one-shot multivibrators, etc.

The Advantages of MECL

1. Highest speed IC logic available
2. Low cost
3. Low output impedance

4. High fanout capability
5. Constant supply current as a function of frequency or logic state
6. Very low noise generation
7. Complementary logic outputs save on package count
8. Low crosstalk between signal leads
9. All outputs are buffered
10. Outputs can be tied together giving the Implied-OR function
11. Common mode rejection of noise and supply variations is 1 V or greater for differential line receiving
12. Bias supplies are internal, allowing MECL use with a single power supply
13. Minimal degradation of parameters occurs with temperature variations
14. Large family of devices yields economical designs
15. Power dissipation can be reduced through use of Implied-OR and the "Series Gating" technique
16. Easy data transmission over long distances by using the balanced twisted pair technique with standard parts
17. Constant noise immunity versus temperature
18. Best speed-power product available
19. All positive logic functions are available
20. Adapts easily to MSI and LSI techniques

MECL Areas of Application

1. Instrumentation
2. High speed counters
3. Computers
4. Medical electronics
5. Military systems
6. Large real-time computers
7. Aerospace and communication satellite systems
8. Ground support system
9. High speed A/D conversion
10. Digital communication systems
11. Data transmission (twisted pair)
12. Frequency synthesizers
13. Phase array radar
14. High speed memories
15. Data delay lines

Purpose of This Book

Rules and guidelines for using the various MECL families comprise the subject matter of this book. Because of edge speed and bit rate capabilities, each family has differing system requirements. The family name will therefore be referenced for the examples and figures in the text, whenever applicable. The information in this book is meant to apply to MECL II, MECL III, and MECL 10,000. The information about MECL II will generally apply to MECL I, although the data would be conservative because of the slower MECL I speed. This book aims at giving the reader an understanding of the MECL families, as well as the knowledge needed to confidently design with and use MECL.

Chapter 1 discusses the operation of MECL circuits and the characteristics of the various families. It also shows methods for internally connecting the basic gates to provide efficient complex functions. Of more importance to the user is Chapter 2 – a list of rules providing a condensed reference for *using* the various MECL families.

Chapters 3, 4, 5, and 6 elaborate on those rules giving a technical background for good system design and presenting test results showing MECL circuits in various modes of operation. Chapter 3 describes circuit-to-circuit interconnections on a card. Both open wire and transmission line techniques are covered. Chapter 4 expands the wiring techniques to show methods for card-to-card and panel-to-panel interconnections. Chapter 5 elaborates on power distribution, showing how voltage drops and power line noise affect noise immunity. Chapter 6 discusses thermal considerations. Attention is given to the problems of calculating chip temperature, removing heat from the system, and to the effect of thermal differences on noise immunity.

Chapter 7 provides background necessary for understanding transmission lines as they apply to MECL. Derivations of equations are shown, along with test results correlating with the theoretical analysis. This chapter should be especially useful when selecting a transmission line impedance and when determining the effect of fanout or stray capacitance on the line.

Chapter 8 contains application ideas for MECL circuits. Included are methods for interfacing various logic families with MECL, and numerous useful circuits designed with MECL for high performance.

Chapter 9 discusses ac noise immunity characteristics exhibited by MECL 10,000 devices, and describes methods for testing circuit performance when subjected to electrical noise.

In Chapter 10 is contained a short discussion of the system use of MECL 10,000 devices designed for use over the military temperature range.

Finally, a brief appendix illustrates some of the peripheral hardware and components of use in MECL Systems.

CHAPTER 1 MECL Families

The Basic MECL Gate

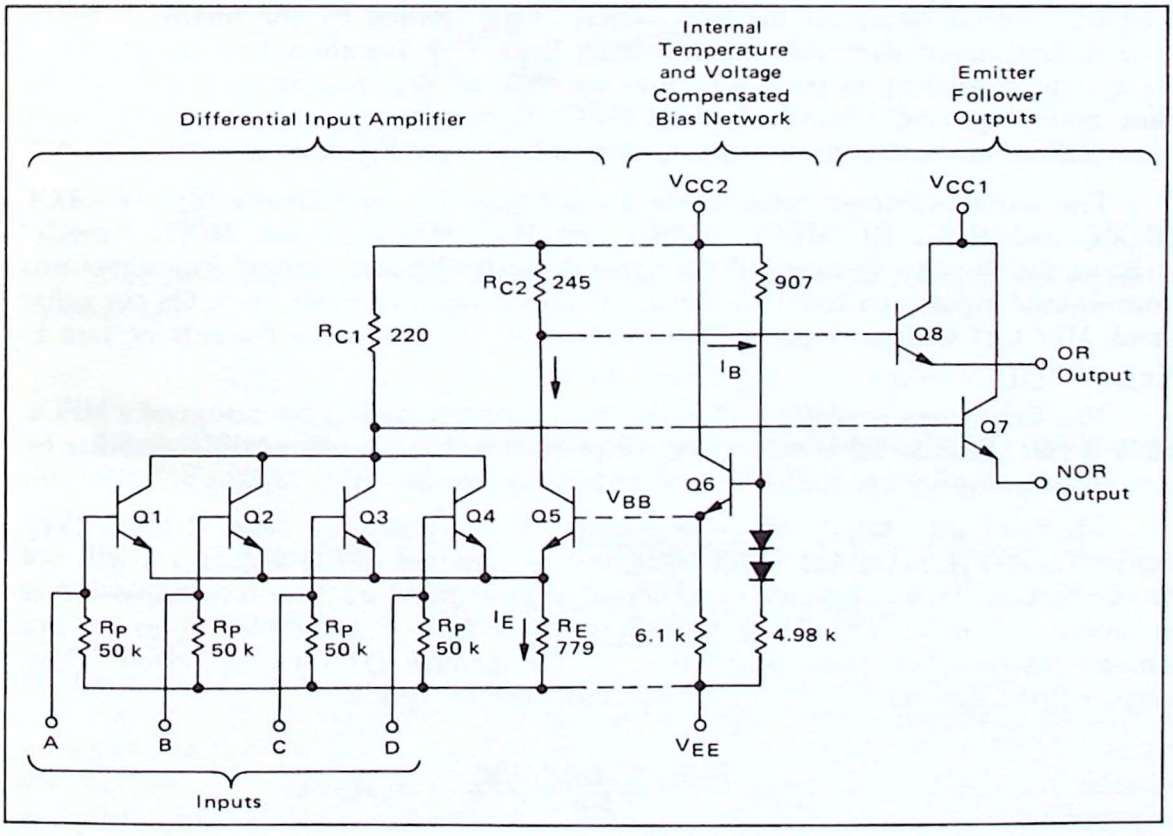
An understanding of the basic circuits used in the construction of a logic family is important in order to successfully design and trouble-shoot a system which uses the family. This chapter describes MECL circuits, compares MECL families, and gives some suggested rules for using MECL circuits in system design.

Figure 1-1 shows a typical MECL gate, – the basic gate circuit for the MECL 10,000 family. (Similar schematics are provided for each other MECL logic family, in the general information section of the MECL Data Book). The figure shows the separate functional circuits within the gate.

The differential amplifier section contains the current steering element that provides the actual logic gating of the circuit. It also provides the voltage gain necessary for a narrow linear threshold region.

An internal temperature and voltage compensated bias driver supplies a reference voltage for the differential amplifier. The bias voltage, V_{BB}, is set at the midpoint of the signal logic swing. With the recommended -5.2 volts supply voltage

1-1: MECL 10,000 Basic Gate



and 25°C ambient temperature, V_{BB} is -1.29 volts dc for either MECL 10,000 or MECL III, and -1.175 volts dc for MECL II. The diodes in the voltage divider line, together with Q6, provide temperature compensation by maintaining a level consistent with the midpoint of the logic levels despite changing temperatures.

One additional feature of the bias supply is its ability to track supply voltage changes. Consequently MECL II gates, for example, are specified to operate from a -5.2 volt ±20% supply. In fact, they are capable of working over a much wider range (-3.0 to -8.0 volts) although ac performance would be degraded.

The emitter followers are output drivers. They provide level shifting from the differential amplifier to MECL output levels, and provide a low output impedance for driving transmission lines. Both MECL 10,000 and MECL III circuits use open emitter outputs. The reason is that since these circuits are designed for use with transmission lines, and since the line termination provides an output load, internal pulldown resistors would be a waste of power.

However MECL II, which is not specified to drive transmission lines, offers gates both with and without pulldown resistors. In general, the circuits without pulldown resistors are intended for use in Wired-OR circuit designs rather than for driving high fanout loads. MECL II circuits with internal output pulldown resistors use 1.5 kΩ values for standard speed parts, and as low as 600 Ω values for the high speed circuits.

MECL 10,000 and MECL III circuit families, designed to drive transmission lines, have two V_{CC} power voltage inputs. V_{CC1} is used to supply current to the output drivers, while V_{CC2} supplies the remainder of the circuit. Separate V_{CC} lines are used to eliminate crosstalk between circuits in a package. More important, the use of two lines speeds up circuit performance by eliminating a voltage spike which otherwise would occur on the bias voltage, V_{BB}, caused by the relatively heavy currents associated with transmission lines. Each V_{CC} pin should be connected to the system ground by as short a path as possible (all V_{CC} pins are connected to the same system ground). Standard speed MECL II circuits are not designed to drive transmission lines and consequently require only a single V_{CC} package pin.

The input pulldown resistors shown in Figure 1-1 are characteristic of MECL 10,000 and MECL III. MECL 10,000 and Hi-Z MECL III use 50 kΩ "pinch" resistors which serve to drain off the input transistor leakage current. These resistors hold unused inputs at a fixed zero level, so unused inputs are left open. On the other hand, MECL II without input pulldown resistors, requires unused inputs be tied to V_{EE} or V_{OL}.

The following calculations illustrate the current switching operation of a MECL 10,000 gate. Similar calculations may be performed for the other MECL families by substituting appropriate resistor values and voltage levels.

When all gate inputs are at a voltage, V_{in}, equal to a logic ∅ level, $|V_{IL}\ \text{min}| \geq |V_{in}| \geq |V_{IL}\ \text{max}|$, the input transistors Q1 through Q4 in Figure 1-1 will not be conducting current, because the common emitter point of these four transistors is at about -2.09 V: i.e., $V_{BB} + V_{BEQ5} \approx -1.29\ V + (-0.80\ V)$. This is not enough forward bias (base to emitter) on Q1 through Q4 for conduction. Thus, current flows through R_{C2}, Q5, and R_E. This current, $I_{E\emptyset}$, is:

$$I_{E\emptyset} = \frac{V_{EE} - (V_{BB} + V_{BE})}{R_E} \approx -4.0\ \text{mA}.$$

The voltage drop at the collector resistor. R_{C2}, may be calculated as:

$$V_{RC2} = I_{E\emptyset}R_{C2} + I_B R_{C2} \approx (-4.0\ \text{mA}) \bullet (245\ \Omega) = -0.98\text{V}.$$

The output transistor base current, I_B, is small compared to the switch current, so the second term above can be ignored.

The OR output is then obtained through an emitter-follower, Q8, which cuts the output level by one base-emitter drop, giving a voltage level:

$$V_{OL\ OR} = V_{RC2} + V_{BE},$$

where: V_{BE} = base to emitter drop on Q8, with logic zero current level (i.e., 6 mA thru Q8).

So:

$$V_{OL\ OR} \approx -0.98\ \text{V} + (-0.77\ \text{V}) \approx -1.75\ \text{V},$$

typical at $T_A = 25°\text{C}$.

The base of the NOR output emitter-follower, Q7, is at about -0.05 V, yielding an output of -0.924 V typical, at an output device current level of 22.5 mA and $T_A = 25°\text{C}$. (These output voltage and current levels assume 50-ohm loads to a terminating voltage, V_{TT}, of -2.0 V).

If one or more of the gate inputs is switched to a voltage level, V_{in}, equal to a nominal logic 1 level, $|V_{IH\ min}| \geqslant |V_{in}| \geqslant |V_{IH\ max}|$, a current I_{E1} flows through R_{C1}, Q1-Q4, and R_E. This current is:

$$I_{E1} = \frac{V_{EE} - (V_{in} + V_{BE})}{R_E} \approx -4.49\ \text{mA},$$

where: $V_{in} = -0.924\ \text{V}$

$V_{BE} = -0.79\ \text{V}.$

The current flow through R_{C1} produces a voltage at the collector nodes of Q1 through Q4:

$$V_{RC1} \approx I_{E1}R_{C1} = (-4.49\ \text{mA}) \bullet (220\ \Omega) \approx -0.98\ \text{V}.$$

Finally, the output is obtained through an emitter follower, Q7, which drops the collector voltage level one base-emitter drop, so that:

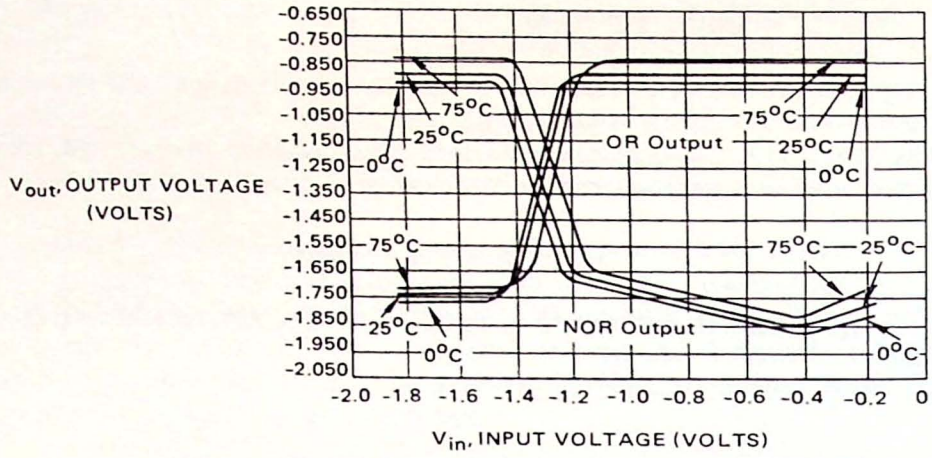
$$V_{OL\ NOR} = V_{RC1} + V_{BE}\ (\text{output device at 6 mA})$$

$$\approx -0.98\ \text{V} + (-0.77\ \text{V}) = -1.75\ \text{V},$$

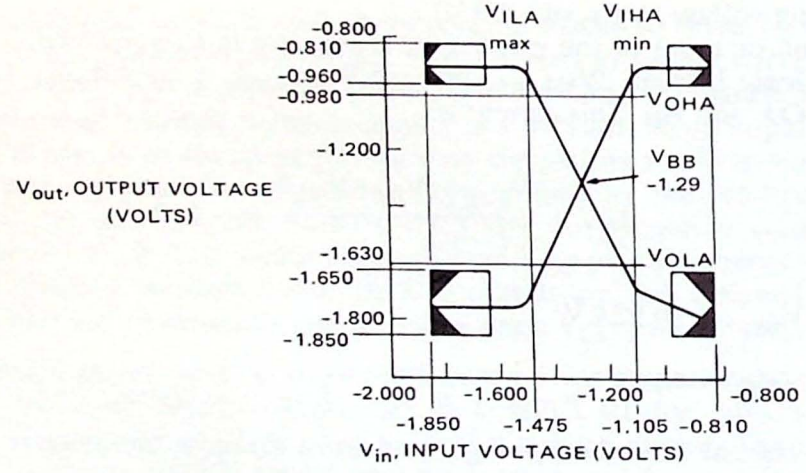
typical at $T_A = 25°\text{C}$.

The transfer curves in Figures 1-2(a) and (b) indicate the behavior of the MECL gate while switching. Note from the data in Figure 1-3 and from the NOR transfer characteristic: for V_{in} increasing from $V_{IL\ min}$ to $V_{ILA\ max}$, the output remains at a high level. When V_{in} increases from $V_{ILA\ max}$ to $V_{IHA\ min}$, the NOR output

1-2: MECL 10,000 Transfer Characteristics and Specification Points



(a) MECL 10,000 Transfer Characteristics
V_{EE} = 5.2 V



(b) MECL 10,000 Specification Points (25°C)

1-3: MECL 10,000 and MECL III Specified Logic Levels and Thresholds

PARAMETER (VOLTS)	0°C		+25°C		+75°C	
	MECL 10,000	MECL III	MECL 10,000	MECL III	MECL 10,000	MECL III
$V_{IH\ max}$ & $V_{OH\ max}$	-0.850	-0.840	-0.810	-0.810	-0.720	-0.720
$V_{OH\ min}$	-1.010	-1.000	-0.960	-0.960	-0.900	-0.900
$V_{OHA\ min}$	-1.030	-1.020	-0.980	-0.980	-0.920	-0.920
$V_{IHA\ min}$	-1.155	-1.135	-1.105	-1.095	-1.045	-1.035
$V_{ILA\ max}$	-1.485	-1.500	-1.475	-1.485	-1.445	-1.460
$V_{OLA\ max}$	-1.640	-1.615	-1.630	-1.600	-1.600	-1.575
$V_{OL\ max}$	-1.660	-1.635	-1.650	-1.620	-1.620	-1.595
$V_{IL\ min}$ & $V_{OL\ min}$	-1.870	-1.870	-1.850	-1.850	-1.830	-1.830

Conditions: Ceramic DIL package stabilized with ≥500 lfm air flow.

will switch to a low level. Then, as the input continues more positive than $V_{IHA\ min}$, the output continues more negative with a slope of about -0.24. This is caused by the collector input node going more negative because of increasing collector current as V_{in} goes more positive.

If the input continues in the positive direction, saturation will be reached at an input of about -0.4 volts. Beyond that point, the base-collector junction is forward biased to saturation and the collector voltage and output will go more positive with the increasing input level. Since the saturation point is well above $V_{OH\ max}$, operation in this mode will not occur in normal system operation. The OR output level depends on Q5's collector voltage (cf Fig. 1-1). This output is unaffected by input levels except in the active transfer region.

Suffice it to say that while the manufacture of MECL circuits is not a primary concern of the user, nevertheless ease of manufacture does translate directly into end product cost. Although not as easy to build as some slower logic families because of smaller transistor geometries, MECL does have some features which facilitate processing. First, the voltage gain of the basic gate circuit (approximately 4.5 for MECL 10,000) is essentially independent of transistor beta. So transistor beta can be allowed to vary from a low of about 70 in high speed MECL (40 for MECL II) to a high in excess of 300, which permits easy processing limits. Second, the output voltage levels depend on diode drops for a high output, and diode drops and resistor ratios for a low output. Resistance ratios can be held to within ±5% even though absolute values vary by ±20%. Again, this eases processing.

Third, since the transistors used do not saturate, the gold doping which is normally required to decrease storage time is not required in MECL processing; therefore yields are better. Fourth, collector-emitter voltages are low, due to circuit design, again relaxing processing restrictions. Such advantages, together with Motorola's ability to control processing, permit high volume production of all MECL circuits. In effect, this means low-cost high performance circuits for the designer.

Noise Margin

Noise margin is a dc voltage specification which measures the immunity of a circuit to adverse operating conditions. Noise margin is defined as the difference between the worse case input logic level ($V_{IHA\ min}$ or $V_{ILA\ max}$) and the guaranteed worst case output ($V_{OHA\ min}$ or $V_{OLA\ max}$) for those inputs. Figure 1-3 lists the worst case limits for MECL 10,000 and MECL III. (MECL II levels may be found in the general information section of the Motorola "MECL Integrated Circuits Data Book").

High level noise margin is obtained by subtracting ($V_{IHA\ min}$) from ($V_{OHA\ min}$); similarly, low level noise margin is ($V_{ILA\ max}$) minus ($V_{OLA\ max}$). Worst-case noise margin is guaranteed to be at least 0.175 volts for MECL II, 0.125 volts for MECL 10,000 (and MECL III in stud packages), and 0.115 volts for MECL III in dual in-line packages. Using typical output voltage levels for MECL circuits, noise margins are usually better than guaranteed – by about 75 millivolts.

A second noise parameter of interest to the designer is obtained by cascading worst case gates and measuring the minimum "noise" input that will propagate through the gates. This measurement is more indicative of actual system operation than dc noise margin, and is often referred to as "noise immunity" or "ac noise immunity". Testing has shown that this "noise immunity" is typically at least 40 millivolts greater than the dc noise margin specified by voltage levels. However, ac

noise immunity is rather difficult to measure. Consequently it is not specified on the data sheets.

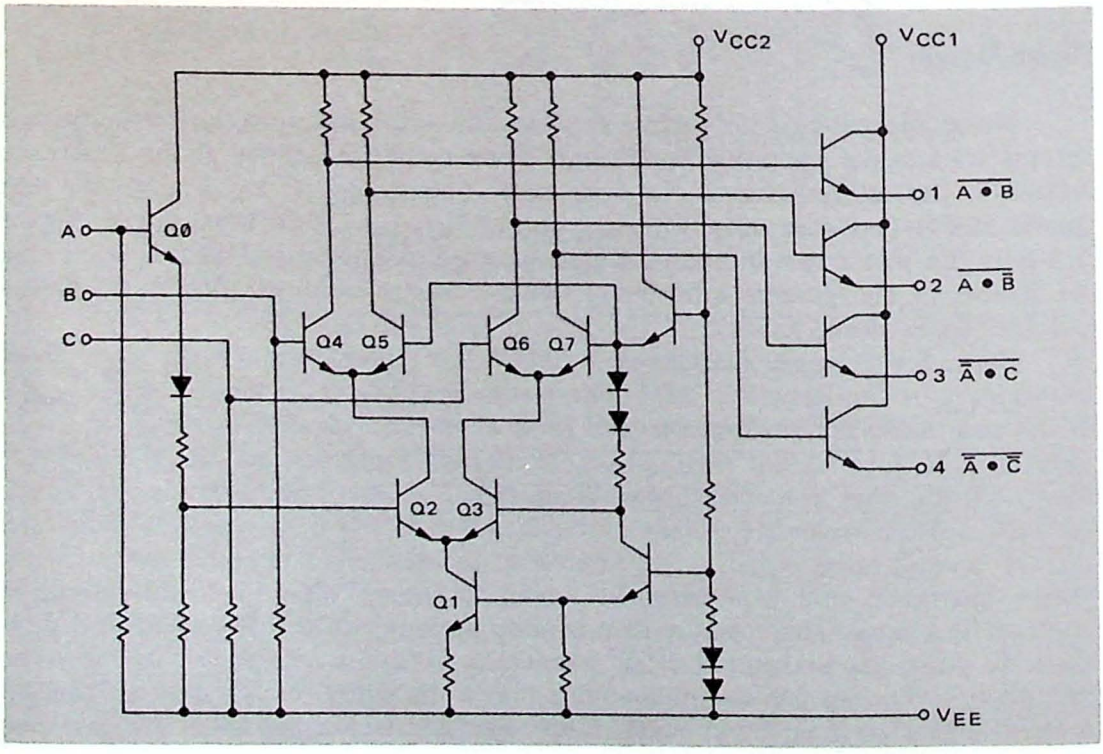
In system design, the user is concerned with noise margin when devices at different temperatures and different power supply voltages interface with each other. Figure 1-3 tabulates the worst case change in logic levels as a function of temperature. Equally important is the change in output levels as a function of supply voltage (cf Figure 5-2). The logic 1 levels are relatively independent of power supply voltage, and the change in the output level is typically less than 0.05 of the V_{EE} change. The change in the $\emptyset$ level is a function of the resistor ratios in the current switch and is typically 0.25 of the V_{EE} change. These values illustrate the rejection of power supply variations that is characteristic of MECL. Detailed information on noise margin changes due to power supply and temperature variations is given in Chapters 5 and 6.

MECL Circuit Types

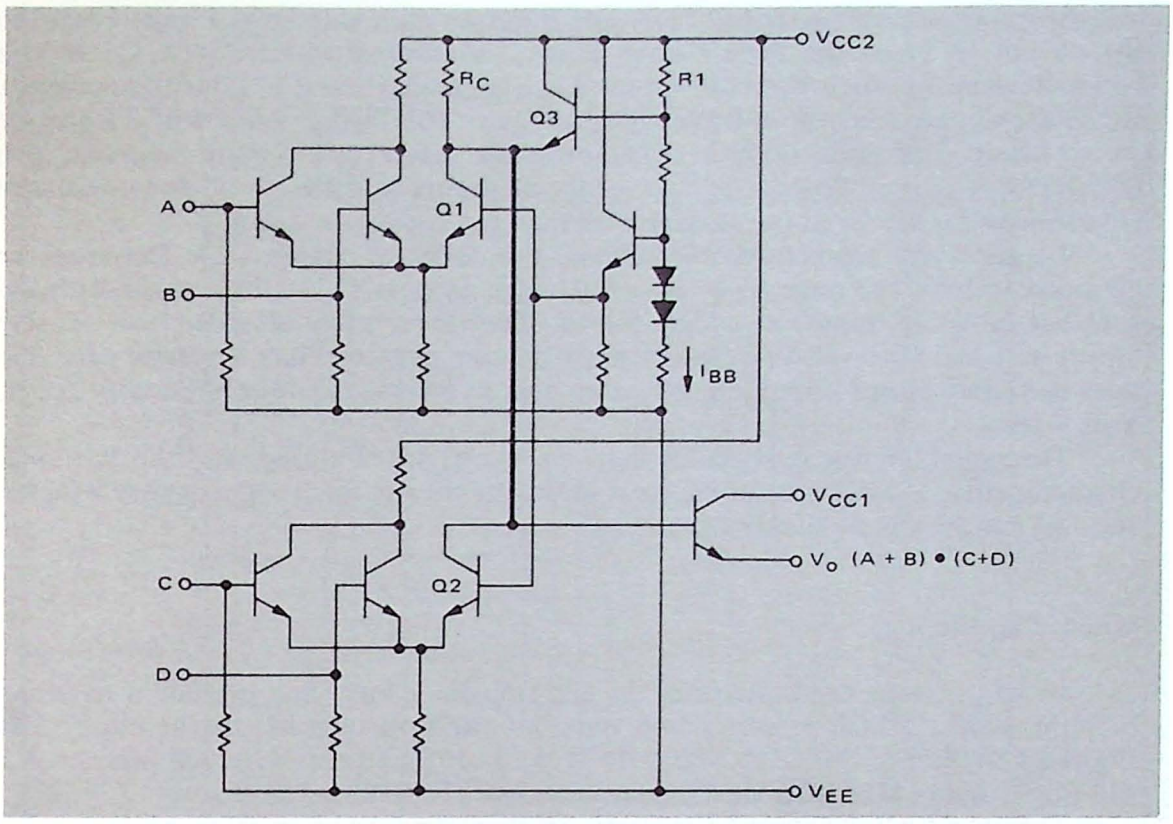
It is possible to connect the basic MECL differential amplifiers together within a circuit to increase logic flexibility, speed, and power efficiency. Two techniques, series gating and collector dotting, add the NAND and AND logic functions to the basic OR and NOR operation of the MECL gate with very little increase in propagation delay. A third technique, Wired-OR, gives the logic OR function by tying together two or more emitter-follower transistors. This is used internally in complex functions to save speed and power and, unlike collector dotting, may also be used externally by connecting logic outputs together.

Series gating is accomplished by connecting MECL differential amplifiers in a current-switch "tree", building up from a current source, Q1, as shown in Figure 1-4. The A input controls the switch, Q2/Q3 through the level shifter Q$\emptyset$ and the

1-4: Series Gating



1-5: Collector Dotting



associated resistor diode network. The bias network is modified to provide the proper voltage level at Q3, a level which is lower than that on Q7 and Q5. The two upper switch pairs are controlled by inputs B and C. The overall circuit generates the four logic functions: $\overline{A \cdot B}$, $\overline{A \cdot \overline{B}}$, $\overline{\overline{A} \cdot C}$, and $\overline{\overline{A} \cdot \overline{C}}$. MECL circuits use up to three levels of series gating, permitting up to eight logic functions with one current source.

The propagation delay from an input, to a top current switch is approximately one gate delay. The propagation delay from an input to a lower level current switch is slightly longer because of the input level shifter QØ. Typically, the latter takes about 1.5 gate delays. More specific information is found on the data sheet for a particular part.

Because of the bias network design, some of the MECL II series gated circuits require unused inputs to be connected to V_{OL} instead of to the normal V_{EE} connection. These circuits are identified by specifying $V_{IL\ min}$ other than -5.2 V on the data sheets.

Series gating is an advantage in MECL logic since it provides the AND or NAND logic functions. Together with the OR/NOR function of the basic gate, MECL has the four basic logic functions needed for efficient logic design. Series gating is used internally in most MECL complex functions and flip flops.

Collector dotting is a second logic technique which is used in the MECL 10,000 series. With it, the logic AND function can be generated by interconnecting one collector node of separate differential current switches as shown in Figure 1-5. When connected this way the two 2-input OR gates give the logic function:

$$V_O = (A + B) \cdot (C + D)$$

Only one collector resistor (R_C) is used for the two transistors Q1 and Q2. The interconnection requires that at least one input to each gate be at a logic 1 level for the output to be at the logic 1 level. Since it is possible to have both Q1 and Q2 conducting at the same time (all inputs low), a clamp is used to limit the current in R_C and maintain the output ∅ logic level voltage. This clamp consists of R1 and Q3. They insure that the Q1/Q2 collector node never goes more negative than ($I_{BB}R_1 + V_{BEQ3}$). Propagation delays for all inputs to collector dotted circuits are equal and are typically about 20% greater than the basic gate delay.

To allow for temperature variations, the collector-dotted logic functions are designed to have the same V_{OL} as normal logic gates at $T_A = 75°C$ when only *one* gate has all of its inputs at a logic ∅ level. Therefore, when *all* gates have all their inputs at a logic ∅ level, V_{OL} wili be slightly more negative than a normal gate. This does not limit device operation, but does give an increase in noise immunity for the logic ∅ level.

The collector dot (OR-AND) logic function, series gating, and the Wired-OR characteristics of MECL combine to provide the means for designing very efficient and fast complex logic functions.

MECL Flip-Flops

In addition to the basic gate, the flip-flops in a logic line provide a necessary building block. MECL employs two types of flip-flop circuits; the ac coupled JK flip-flops found in MECL I and MECL II, and the direct coupled master-slave flip-flops used in MECL II, MECL 10,000 and MECL III.

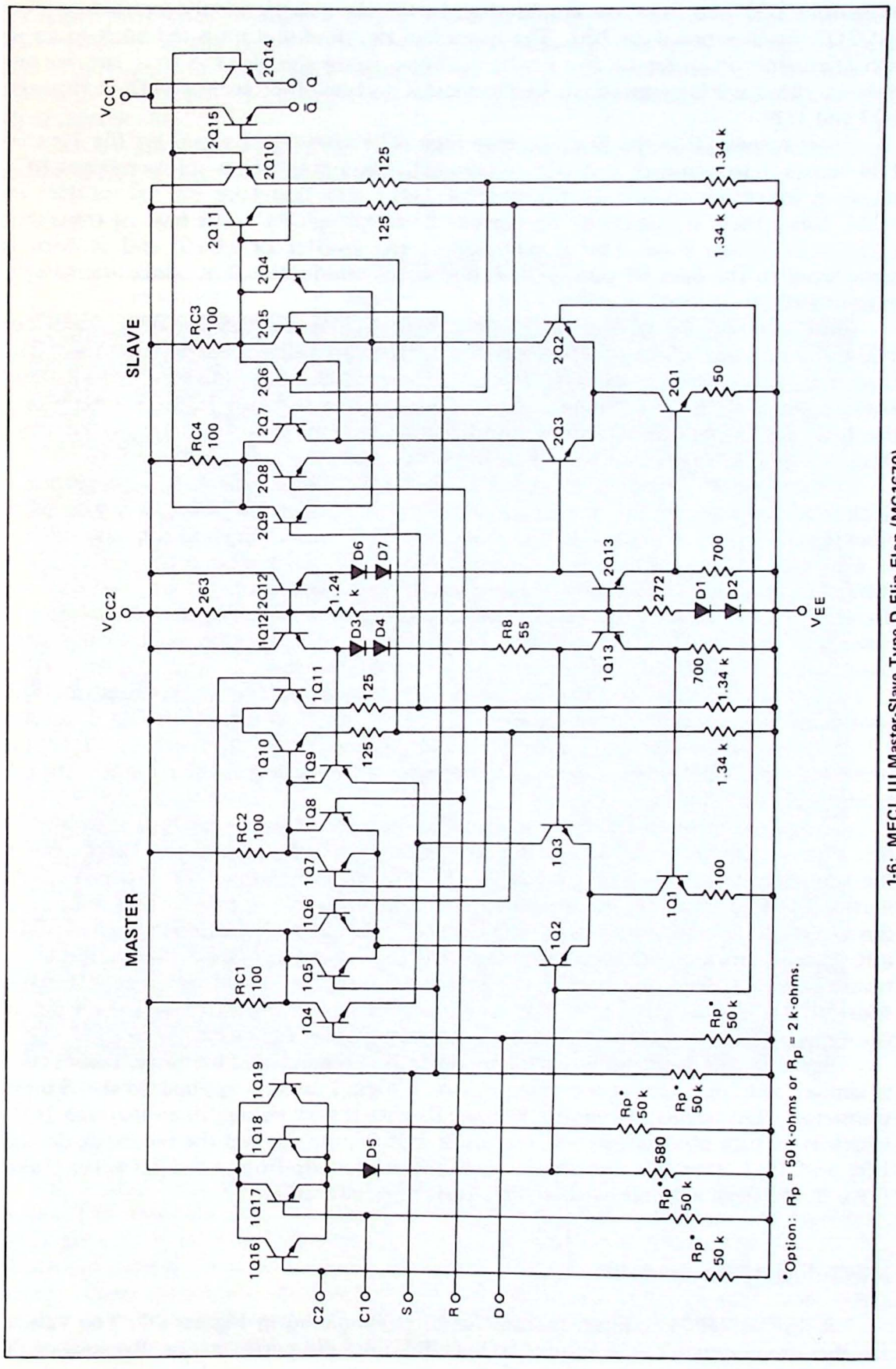
The MECL II ac coupled flip-flops are characterized by small capacitors (25 to 30 pF) coupling the $\overline{J}$ and $\overline{K}$ inputs to the storage section of the circuit. Because of this capacitive coupling, the circuit is somewhat sensitive to input rise time. However, the circuits will trigger on signals of MECL amplitude with edges up to 100 ns long – much longer than any MECL edge. The multiple $\overline{J}$ and $\overline{K}$ inputs of the MC1013/MC1213 and MC1027/MC1227 are especially useful in synchronous counters or counters with non-binary counting sequences.

A limitation on these flip-flop circuits is their susceptibility to some types of noise on the input line. For example, a positive going input with a large overshoot on a $\overline{J}$ input will override a 1 level on another $\overline{J}$ input intended to inhibit that positive going signal. The overshoot will couple through the capacitor and look like a $\overline{J}$ input. A similar condition exists on the $\overline{K}$ inputs. Fortunately the problem is not a serious one and its solution requires only that the input signals do not have excessive ringing. It is recommended that overshoot on the $\overline{J}$ and $\overline{K}$ inputs be held to 100 millivolts.

The MECL II type D, and all MECL 10,000 and MECL III flip-flops, use the direct coupled master-slave circuit as shown in Figure 1-6 for the MC1670. In each direct coupled circuit the master is updated while the clock is low, and data is transferred to the slave on the positive excursion of the clock. This type of circuit offers better noise protection than the ac coupled circuit and is not susceptible to overshoot on the inputs. Also, the master-slave flip-flops do not have the rise time limitations of the ac coupled circuits.

Operation Of Flip-Flop

In the circuit of Figure 1-6 assume that initially Q, C_1, C_2, R, S, and D are at ∅ levels and that $\overline{Q}$ is at the 1 level. Since the clocks and the R and S inputs are low,



1-6: MECL III Master-Slave Type D Flip-Flop (MC1670)

transistors 1Q3 and 2Q3 are conducting. In the slave section only transistors 2Q6 and 2Q7 are in series with 2Q3. The output of the slave section is fed back to these two transistors in order to form a latch. Thus, when the clock is low, the output state of the slave is maintained. In the master section, the current path is through 1Q3 and 1Q9.

Now assume that the D input goes high. The high-input signal on the base of 1Q4 causes it to conduct, and 1Q9 to turn off. The voltage drop across resistor RC1 causes a low-state voltage on the base of 1Q11 and therefore on the emitter of 1Q11. Since there is essentially no current flow through RC2, the base of transistor 1Q10 is in a high state. This is reflected in the emitter of 1Q10, and in turn is transferred to the base of 1Q6. 1Q6 is biased for conduction but, since there is no current path, it does not conduct.

Now assume one of the clocks goes high. As the clock signal rises, transistor 1Q2 turns on and transistor 1Q3 turns off. This provides a current path for the common-emitter transistors 1Q5, 1Q6, 1Q7, and 1Q8. Since the bases of all these devices except 1Q6 are in the low state, current flow is through 1Q6. This maintains the base and emitter of 1Q11 low, and the base and emitter of 1Q10 high. The high state on 1Q10 is transferred to 2Q4 of the slave section.

As the clock continues to rise 2Q2 begins to turn on and 2Q3 to turn off. (Reference voltages in the master and slave units are slightly offset to insure prior clocking of the master section). With transistor 2Q2 conducting and the base of 2Q4 in a high state, the current path now includes 2Q2, 2Q4, and resistor RC3. The voltage drop across the resistor places a low-state voltage on the base of 2Q11, and therefore on the emitter, of 2Q11. The lack of current flow through RC4 causes a high-state input to the base of 2Q10. Finally these states are fed back to the latch transistors, 2Q6 and 2Q7 and appear on the Q and $\overline{Q}$ outputs.

As the clock voltage falls, transistor 2Q2 turns off and 2Q3 turns on. This provides a current path through the latch transistors, "locking in" the slave output.

In the master section, the falling clock voltage turns on transistor 1Q3 and turns off 1Q2. This enables the input transistor 1Q4 so that the master section will again track the D input.

A separation of thresholds between the master and slave flip-flops is caused by R8. The current through this resistor produces an offset between the thresholds of the transistor pairs 1Q2/1Q3 and 2Q2/2Q3. This offset disables the D input of the master flip-flop prior to the enabling of the information transfer from master to slave via transistors 2Q4 and 2Q9. This disabling operation prevents false information from being transferred directly from master to slave during the clock transition, particularly likely if the D input changes at this time. The offsetting resistor, R8, also allows a relatively slow-rising clock waveform to be used without the danger of losing information during the transition of the clock.

Both set and reset inputs are symmetrically connected. Therefore, their action is similar although results are opposite. As a logic 1 level is applied to the S input transistor, 1Q2 begins to conduct because its base is now being driven through 1Q19 which is in turn connected to S. Transistor 1Q5 is now on, and the feedback devices 1Q6 and 1Q7 latch this information into the master flip-flop. A similar action takes place in the slave with transistors 2Q2, 2Q5, 2Q6, and 2Q7.

MECL Family Comparison

A list of MECL circuit characteristics is tabulated in Figure 1-7. The various families are compared with respect to both features and performance. Because of the

big speed difference between standard MECL II and the higher speed MECL II clock drivers, many of the figures in the MECL II column do not apply to the complete line. The following paragraphs describe the MECL characteristics in the order of Figure 1-7. Differences between standard and high-speed MECL II are pointed out when significant.

1-4. . . The first four items in Figure 1-7 are self-explanatory and have been discussed in the introduction and the preceeding section on the basic gate.

1-7: MECL Family Comparison

FEATURE	MECL I	MECL II	MECL 10,000	MECL III
1. Year Introduced	1962	1966	1971	1968
2. Bias Driver Source	MC304/354	Internal	Internal	Internal
3. Output Pulldown Resistors	Yes	Optional	No	No
4. Input Pulldown Resistors	No	No	50 k-ohm	2 k & 50 k-ohm
5. Maximum Input D.C. Loading Current	100 μA	100 μA	240 μA	350 μA
6. Specified Output Current	2.5 mA	2.5 mA	≈22 mA	≈22 mA
7. Maximum Output Current	20 mA	20 mA	40 mA	40 mA
8. Transmission Line Capability	No	No	Yes	Yes
9. D.C. Loading Fan-Out	25	25	92	63
10. Input Capacitance	3.6 pF	3.6 pF	2.9 pF	3.3 pF
11. Output Impedance	22 ohm	15 ohm	7 ohm	5 ohm
12. Gate Propagation Delay	8 ns	4 ns	2 ns	1 ns
13. Gate Edge Speed	8.5 ns	4 ns	3.5 ns	1 ns
14. Flip-Flop Toggle Speed	30 MHz	180 MHz	125 MHz	500MHz
15. Gate Power	31 mW	22 mW	25 mW	60 mW
16. Open Wire Length (Less Than 100 mV Undershoot)	18"	12"	6"	1"
17. Wire-Wrap Capability	Yes	Yes	Yes	No
18. Use of Series Damping Resistors	Yes	Yes	Yes	Hi-Z Only
19. Separate V_{CC} Inputs	No	No	Yes	Yes
20. Speed-Power Product	250 pJ	88 pJ	50 pJ	60 pJ
21. Wired-Or Capability	Yes	Yes	Yes	Yes
22. Full Military Temperature Range	Yes	Yes	No	No
23. Flat-Package	Yes	Yes	Yes	No
24. Dual In-Line Package	No	Yes	Yes	Yes
25. TO-5 Package	Yes	No	No	No

•-30°C to +85°C

5. . . Maximum input dc loading current is specified on individual circuit data sheets. The numbers listed here apply to a single input of a basic gate. If a package input goes to more than one point in a circuit, such as a gate strobe line would, additional current may be required. Because of higher power in the MECL II clock drivers, these inputs are specified at 300 μA maximum input current. The input current difference between the MECL II and MECL 10,000 circuits is due to the 50 kΩ input resistor used with MECL 10,000.

Calculating the input current, I_{in}, for MECL 10,000 with a worst-case input resistor value of 30 kΩ (R_{in}) gives an input resistor current of:

$$I_{in} = \frac{V_R}{R_{in}} = 143\ \mu A$$

$$V_R = |V_{EE} - V_1| = 4.3\ V,$$

where: V_R = voltage drop across the input resistor, R_{in}, with a logic 1 input,

V_{EE} = −5.2 V supply voltage,

V_1 = −0.9 V (a typical logic 1 level).

The typical 50 kΩ value will use slightly less current, but either resistance value is very high compared to the output circuit impedance or the line impedance. The 350 μA specification for MECL III applies only to the Hi-Z circuits. The 2 kΩ input impedance of the Lo-Z circuits requires an additional input current of:

$$\frac{V_R}{R_{in}} = \frac{4.3\ V}{2\ k\Omega} = 2.15\ mA.$$

6-8... Output voltage levels are specified at currents representative of circuit operation. MECL I and MECL II are normally used with unterminated lines and are specified for a fanout of 25, i.e., 2.5 mA total output current. Although the MECL II line driver will drive transmission lines, the output levels are given at 2.5 mA to maintain consistency with the rest of the MECL II family. MECL 10,000 and MECL III are designed to drive 50 Ω transmission lines terminated to −2 Vdc (measured from V_{CC}). The current, I_{TT}, required by the line termination is:

$$I_{TT} = \frac{V_{TT} - V_1}{Z_o} = \frac{(-2.0 + 0.9)\ V}{50\ \Omega} = -22\ mA.$$

Consequently, the outputs are specified with 50 ohm loads. The maximum permissible output currents of 20 mA for MECL I and MECL II, 50 mA for MECL 10,000, and 40mA for MECL III, insure a good safety margin over the specified currents.

9... The dc loading fanouts for MECL 10,000 and MECL III are computed by dividing the output current by the input current. However, both ac limitations and current needed in the transmission line termination can be expected to restrict the system fanout to a smaller number than the one computed.

10... Two techniques are used to measure circuit input capacitance. One method uses an impedance meter, such as the H.P. 4815A RF Vector Impedance Meter, to measure impedance and phase angle. The other technique uses a time domain reflectometer (TDR) to measure the effect of capacitance on the impedance of a transmission line. (The mathematical relationships used to calculate input capacitance from TDR data are presented later in Chapter 7). Although small, the

input capacitance will affect system rise time and transmission line propagation delay as a function of fanout at high MECL speeds.

11. . . DC output impedance can be calculated from measurements of the output voltage as a function of output current: $Z = \Delta V/\Delta I$. The gate output impedance must be much lower than the line characteristic impedance in order to provide full MECL signal levels when driving transmission lines. The output impedance (resistive load) is the parallel value of the output transistor and pulldown resistor. It should be noted that capacitance charging rate during a negative transition is limited by current flow through the pulldown circuit.

12-13. . . Gate propagation delay, edge speed, toggle rate, and power dissipation are standard data sheet information. Propagation delay (t_{pd}) is measured from the 50% amplitude point on the input signal to the 50% amplitude point on the output signal. Normally the edge speed given is measured between the 10 and the 90% amplitude points on the output signal. However, because of the amount of rounding on the upper 10% of the MECL 10,000 edges, this family is specified with 20 to 80% edge speeds for easier correlation. Nevertheless, 3.5 ns is a typical 10 to 90% figure which can be compared with other families.

14. . . Toggle speeds are minimum rates for the flip-flops in a family. MECL II has flip-flops with speed figures ranging from 70 to 180 MHz. The 180 MHz figure listed in the table is for the MC1034, the highest-speed MECL II flip-flop.

15. . . Gate power here is specified for MECL II, MECL 10,000 and MECL III with open emitter outputs. The MECL I power figure is higher since that family is only available *with* output pulldown resistors. MECL II gates with pulldown resistors have specified powers ranging from 29 to 47 mW per gate depending on the number of gates per package which share a bias supply, and on the number of complementary outputs. Gate power for the MECL 10,000 and MECL III gates is specified with open emitter outputs, as is usual with most ECL product lines. The wide variety of output loads – both resistors used with transmission lines and pulldown resistors – makes a power specification under load difficult to define. In a system, the output power is added to the gate power to find total power.

16-17. . . Open wire length and wire wrap usage are a function of edge speed and the propagation velocity of the wire. The distances shown are maxima, selected to give less than 100 mV undershoot at the receiving end of the line with a fanout of one. Additional information on line driving is found in Chapter 3. Wire wrap may be used with all families but MECL III. The 1 ns edges associated with MECL III cause too much reflection from the wire wrap connection to permit practical use. The open wire maximum line lengths still apply when using wire wraps, unless some form of resistor damping or line termination is used.

18. . . Damping resistors consist of small resistors (5 to 75 ohms) that are placed in series with a line at the output of the driving circuit to extend the permissible line length. The resistor provides a closer match between the line and the output impedance of the circuit than a direct connection. This match limits overshoot and ringing, and allows the use of line lengths somewhat greater than twice the non-damped lengths.

This technique is useful with all MECL circuits except low impedance (Lo-Z) MECL III. The reason is that the 2.2 mA input current required by the 2 kΩ input resistor would cause a voltage drop which would impose prohibitive loss of noise margin in the logic 1 state.

19. . . Separate V_{CC} inputs (V_{CC1}, V_{CC2}) are characteristic of MECL 10,000, MECL III, and some of the high speed MECL II circuits. The separate V_{CC} pins are used

to minimize any crosstalk between circuits in a package which might occur with the high switching currents when driving transmission lines. MECL I and MECL II circuits, not designed to be used with transmission lines, have no requirement for separate V_{CC} lines. Separate V_{CC} lines do not affect using the parts and only require that two package pins be connected to a single ground plane or ground bus.

20... Speed-power product is a measure of a logic family's efficiency. Propagation delay (nanoseconds) is multiplied by the gate power dissipation (milliwatts) to get a measure of efficiency in terms of energy (picojoules). It is interesting to note that gate efficiency has improved with each succeeding logic line introduced. The speed-power product is slightly inaccurate because power figures are used which do not include output loading (discussed previously). However, TTL speed-power products can be inaccurate also as they are generally computed for the circuits operating at a low rate. Such figures would be much worse for circuits operating near top switching rates.

21... Wired-OR is a technique used with all MECL circuits to obtain the logic OR function by connecting circuit outputs together. With MECL II a maximum of two output load resistors are recommended per Wired-OR connection to limit output current. When several (more than 5) circuits are connected with Wired-OR outputs, it is possible to get a noise spike on the output if all gates are at a 1 output, and all gates but one are simultaneously changed to a logic $\emptyset$. The noise spike is due to the one gate suddenly having to source the output current previously supplied by the other circuits. The pulse width is normally less than the gate propagation delay and of insufficient amplitude to propagate in the system.

22-25... The remaining family features are self-explanatory. Packaging and temperature range for MECL 10,000 are based on initially introduced circuits. Other configurations are being investigated to meet future requirements.

CHAPTER 2 Using MECL

The design guidelines presented here are intended to assist the MECL user to apply MECL families in a system. The rules listed have been tried out in complete systems with good results. As rise times become less than 3 ns, special design rules must be followed. For rise times of 1.5 ns or shorter, designing with transmission lines is necessary.

MECL II, MECL 10,000, and MECL III logic families are treated separately because of the differences in their capabilities and in design techniques to be used. Reasons for the rules, methods for applying them, and test data are found in the following chapters under associated subjects. High speed MECL II clock drivers and flip-flops are not treated separately and should be used in the manner described for MECL 10,000. Otherwise the faster edges of these MECL II circuits may cause sufficient overshoot and ringing to seriously reduce noise immunity or cause false operation.

1. MECL II Design Rules

The MECL II family of integrated circuits is designed to provide high circuit speed without special system layout techniques. This feature simplifies design with this form of emitter coupled logic because most of the techniques used with saturated logic apply to MECL II. The ability of MECL II to interface with the faster MECL 10,000 and MECL III families enables MECL II to be used in slower sections of very high speed systems to gain power economy, eased layout rules, and a large choice of logic functions.

Since MECL II rise, fall, and propagation delay times are typically each 4 ns, transmission line techniques are not required. Standard double-sided circuit boards and backplane wiring are normally used with MECL II.

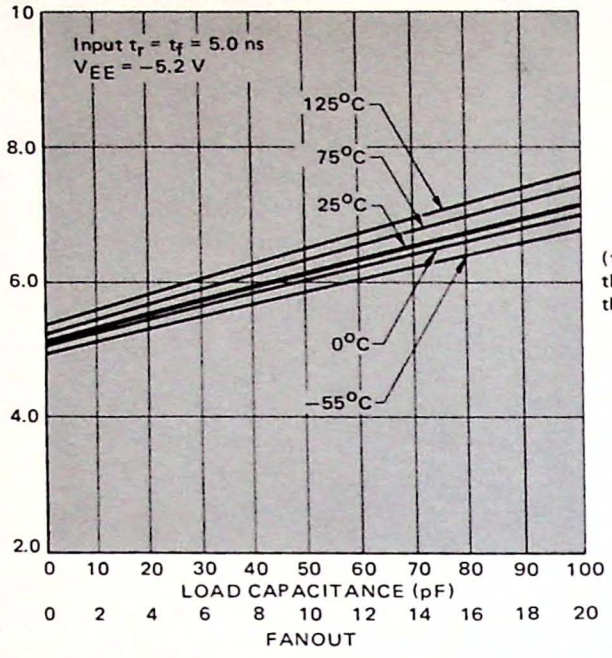
Because of the wide variety of MECL II system sizes and interfaces, not all techniques will apply to every system. The designer should use these rules as guides, modifying them sensibly as required by his particular system.

A. *Logic Design Considerations*

1. MECL rise, fall, and propagation delay times are a function of fanout and capacitive loading. Figures 2-1 through 2-4 show the reduction in speeds with load for MECL II. Consequently, when MECL II is operating near its upper speed limit, fanout should be restricted as indicated by the curves. Because of the emitter follower outputs, fall time and propagation delay to a $\emptyset$ level is more affected by capacitive loading than rise time and propagation delay to a 1 level (note that the curves in Figure 2-4 are steeper than those in Figure 2-3).

2. Fall time and t_{pd-} may be improved by adding a load resistor between the output and -5.2 Vdc. A 1.8 kΩ resistor will cut the delay caused by capacitive

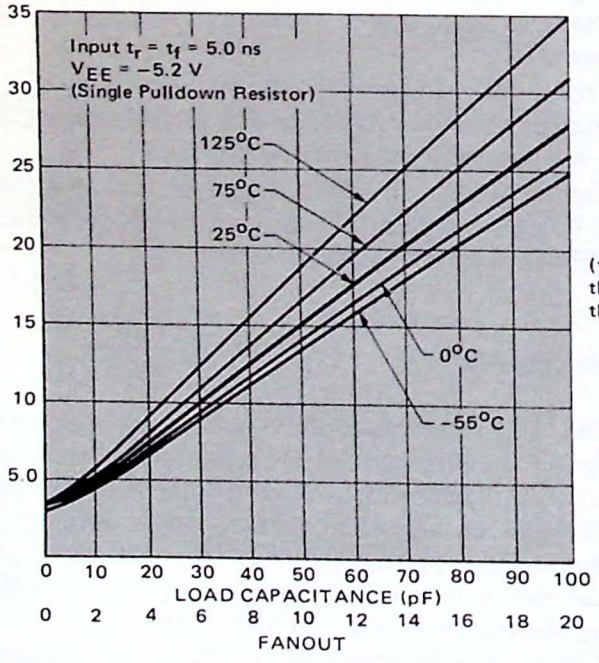
2-1: Rise Time versus Loading and Temperature



t_r, RISE TIME (ns)

(t_r is measured between the 10 and 90% points of the rising edge)

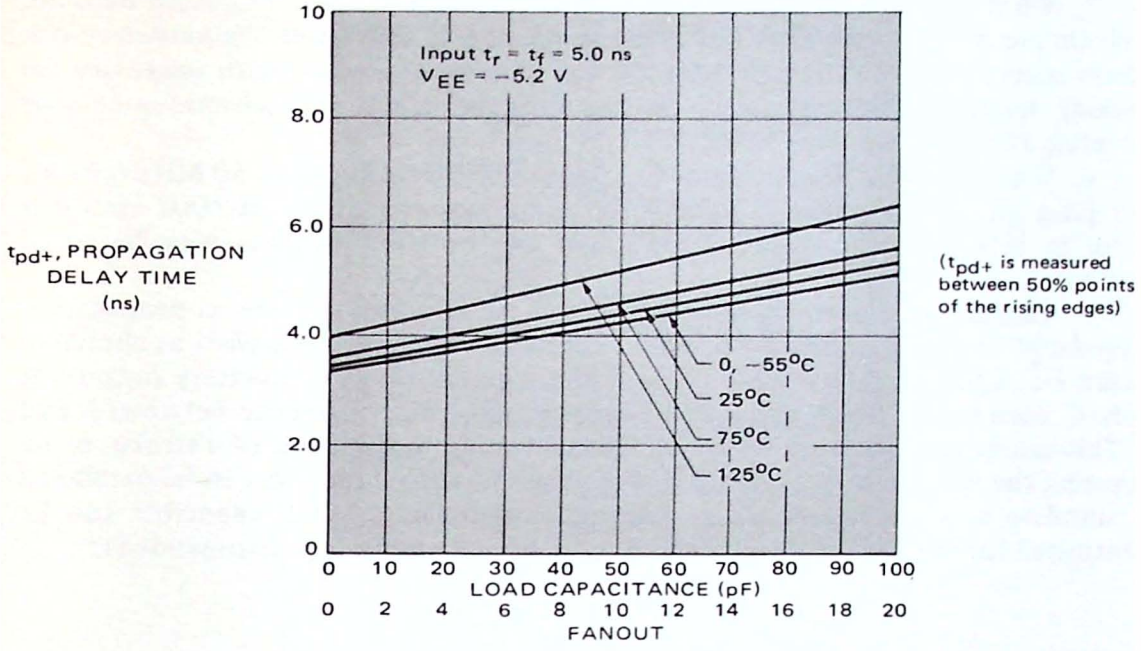
2-2: Fall Time versus Loading and Temperature
(Single Pulldown Resistor)



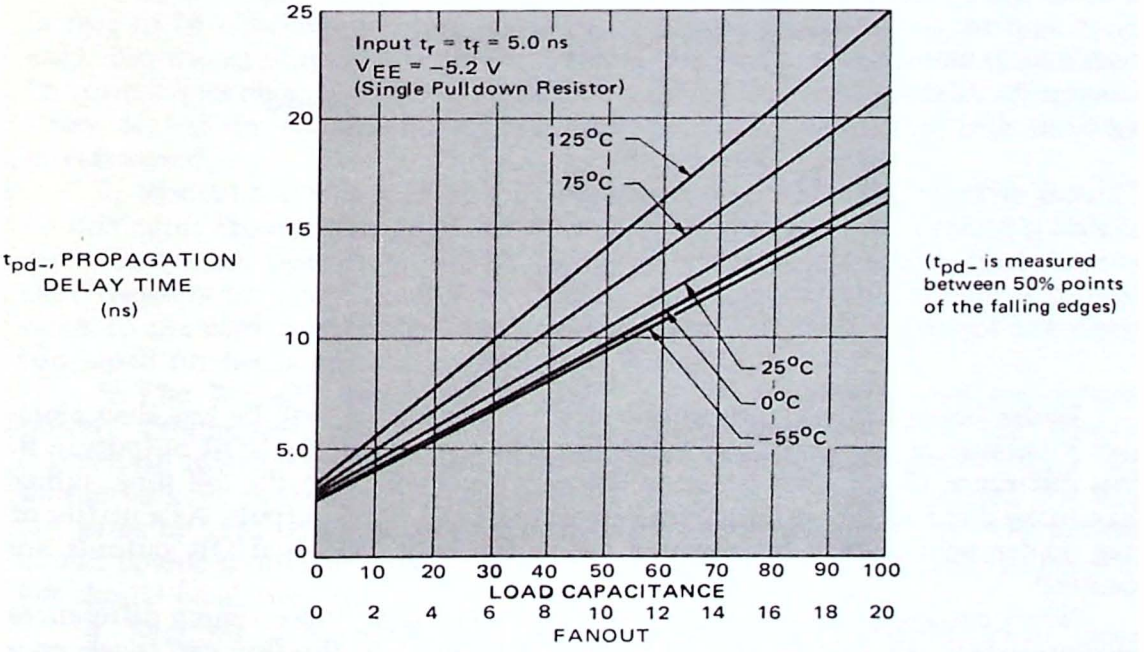
t_f, FALL TIME (ns)

(t_f is measured between the 10 and 90% points of the falling edge)

2-3: Propagation Delay t_{pd+} versus Loading and Temperature



2-4: Propagation Delay t_{pd-} versus Loading and Temperature



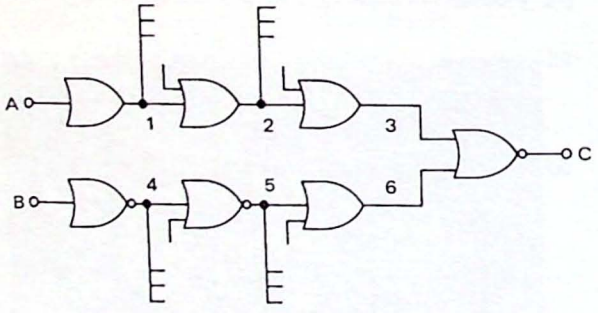
loading nearly in half. Load resistors less than 1.8 kΩ and any load resistors with fanout greater than 10 should be avoided when using circuits with internal pulldown resistors. There may be a reduction in noise immunity when the output is in the 1 state, due to increased output emitter-follower V_{BE} drop.

3. When driving flip-flops at high speed, clock driver circuits should be used. Such circuits are about twice as fast as the standard MECL II gates. As a result, clock drivers such as the MC1023 or MC1026 can provide the bandwidth necessary for clocking several flip-flops at once – as in a shift register or a synchronous counter operating at high speed.

4. When driving a long string of flip-flops at speeds lower than 50 MHz (clock), two gates may be operated in parallel for additional drive. The MC1001 circuit is useful in this application since its multiple OR or NOR outputs may be wired together.

5. The high operating speed of MECL and the effect of loading on propagation delay must be considered when parallel circuits converge at one point, as shown in Figure 2-5. Unequal delays along paths A and B can result in momentary outputs at point C, each lasting a time equal to the propagation delay difference between A and B. This can be compensated for by additional timing in the form of a strobe, or by adjusting the fanouts along A and B. If possible, unused gate inputs can be paralleled to simulate a larger fanout where required; otherwise a small capacitor can be substituted for the needed fanout (about 5 pF per gate input is recommended).

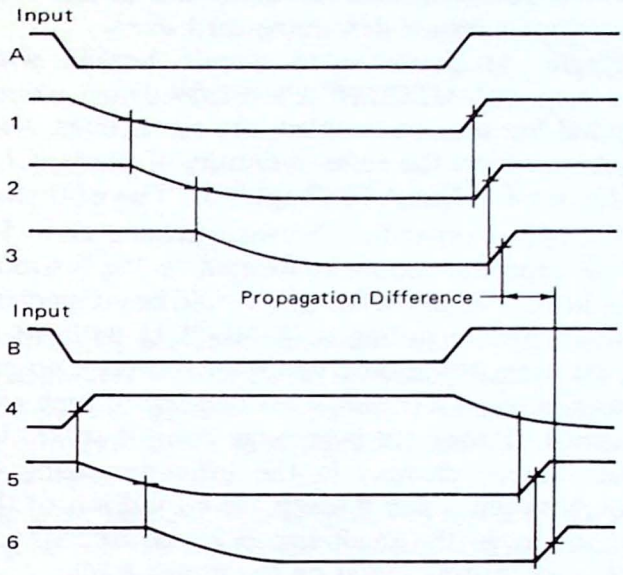
2-5: Parallel Signal Paths



Under heavy loading, propagation delay along path A will be less than along path B because of the use of OR outputs in A as opposed to the NOR outputs in B. This difference (Figure 2-6) is due to the effect of loading on the fall time, rather than being due to a timing difference between OR and NOR outputs. As a matter of fact, under light loading, propagation delays for both NOR and OR outputs are identical.

When designing clocks for the high speed flip-flops, these timing differences become increasingly important. For example, the MC1034 flip-flop can toggle on a 2.5 ns pulsewidth clock. Consequently, timing chain skewing in the order of 2.5 ns can cause false operation.

2-6: Propagation Differences



B. *System Layout Considerations*

1. System grounding and propagation delays in interconnecting leads are factors to be considered before laying out a system. Depending on the type of wire used, the wiring propagation time of a signal can greatly affect overall system speed. In normal backplane wiring it is realistic to expect a 2 ns per foot delay. Propagation delay is less in coaxial cable, but more for signal conductors in a multilayer circuit board.

2. System sections such as shift registers and synchronous counters should be on one card. Propagation delay between shift register clocks on separate boards can cause erroneous operation. Where timing is critical, equal length clock lines (to shift registers or other circuits on separate cards) should be run from a common clock to the card connectors. Such lines will also help limit overshoot and ringing (discussed further in section D, "Backplane Wiring").

3. The Wire-OR capability of MECL can be a powerful tool for reducing power, propagation delay, and package count. However, since the Wire-OR connection switches current when in operation (2.5 mA per load resistor), these leads should be kept as short as possible to avoid crosstalk. It is recommended that Wire-OR gates be kept within a package or between nearby packages. Wire-OR between circuit boards should be avoided. An increased propagation delay of 0.5 ns per Wire-OR should be allowed for.

4. Sections of a system where high fanout may be necessary (such as adders with lookahead carry) should be kept on one card. Signal path length should be reduced as fanout is increased to minimize both line delay and reflections.

C. *Circuit Board Layout Techniques*

1. The size of a MECL II system circuit board is not restricted by the logic family. System requirements should determine card size.

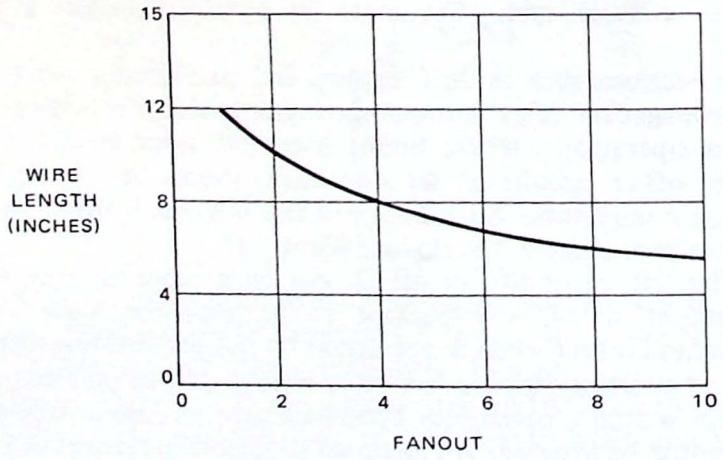
2. Standard single- or double-sided circuit boards with a good ground distribution may be used with MECL II. A low impedance ground is necessary since any noise on the ground line may be coupled into signal lines. Also, any voltage drop across ground will subtract from the noise immunity of the MECL II circuits. Grounding techniques are discussed at length in Chapter 5, "Power Distribution".

3. As with TTL, bypass capacitors, between ground and -5.2 V should be used with MECL. A 1.0 μF capacitor should be located on the board at the power supply inputs. Bypass capacitors, 0.01 μF to 0.1 μF, should be connected-in once every four or five packages. When breadboarding with MECL II without an effective ground bus, an 0.1 μF bypass capacitor should be used for every two packages. RF quality capacitors (low inductance) are recommended because of high circuit speeds.

Unlike TTL, MECL II does not have large current spikes in the circuit during switching, nor large current changes in the interconnecting circuit board paths during the transition between 1 and Ø levels. The function of the bypass capacitors during switching is to charge the small circuit input capacitance and circuit board stray capacitance, thus preventing spikes on the power leads.

4. As with any high speed system, signal lines should be kept as short as possible to minimize ringing and overshoot, as well to simplify timing considerations arising from the propagation delay of a signal along a conductor. Ringing and overshoot are due to the intrinsic inductance and capacitance of the line itself, as well as lumped capacitance at the end of the line. Intrinsic inductance and capacitance are reduced by shortening the lines. A graph of recommended maximum line length as a function of fanout is shown in Figure 2-7. Since increased fanout adds capacitance at the end of the line, the line should be shortened as shown by the following curve.

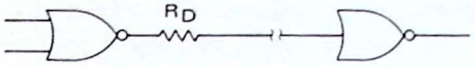
2-7: Recommended Maximum Line Length versus Fanout



5. Longer line lengths are possible if a series damping resistor is used. The resistor is placed at the output of a gate, in series with the signal line as shown in

Figure 2-8. The resistor value depends on the fanout and the required line length. Resistors under 220 ohms for a fanout of one, or under 100 ohms for fanouts

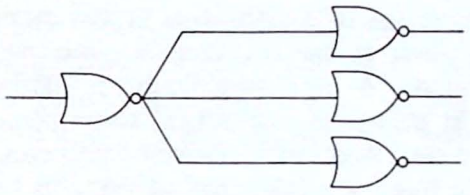
2-8: Damping Resistor



greater than five, are normally used for damping. Values larger than these produce rise and fall time degradation and loss of noise immunity due to IR voltage drop in the resistor. Resistor values are typically 47 ohms, and can be calculated exactly, if desired, from the information given in Chapters 3 and 7. Standard 1/4 watt carbon resistors are commonly used.

6. When driving large fanouts, line lengths can be increased by running parallel leads as shown in Figure 2-9. The distance between the parallel leads is not critical.

2-9: Parallel Signal Paths



This technique should be used for shift register clocks, counter resets, and other high fanout applications. Of course, for synchronous clock lines, clock skew delays should be matched. Series damping may also be used with parallel signal paths.

7. With most MECL II circuits, undershoot ringing on the logic 1 level is critical, since it subtracts from the noise immunity. For safe operating margins, undershoot should be limited to 150 mV. Exceptions to this rule are the MC1013, MC1027, and MC1032 ac coupled flip-flops. Because of their ac coupling, *overshoot* on the inputs should be limited to 100 mV. Shorter signal leads than shown in Figure 2-7 may be required when driving these circuits. Master-slave flip-flops, such as the MC1022 and MC1034, do not have this limitation and can be used with the same *undershoot* rules as the basic gates.

D. *Backplane Wiring*

1. A ground screen is a good means for running a ground in the backplane wiring. A ground screen is made by connecting heavy bus wires to the connectors in a grid pattern before wiring the signal lines. The ground screen lines are wired both parallel to the connectors (tying to the connector pins), and perpendicular to the connectors (contacting multiple ground pins of each connector). This forms a grid network (cf Figure 5-6) of approximately 1 to 2 inch squares over which signals lines are then located.

2. Ferrite beads may be used in backplane wiring for longer signal runs. The recommended line lengths discussed for circuit cards also apply to backplane wiring. A ferrite bead on a wire limits rise and fall time to about 7 ns by attenuating the high frequency components of the signal. With a bead, lines up to three feet long can be driven without excessive overshoot.

3. Standard backplane wiring techniques are used with MECL II. Both wire wrapped and soldered connections perform well. Point-to-point wiring is recommended instead of a laced harness, to lessen line length and reduce crosstalk.

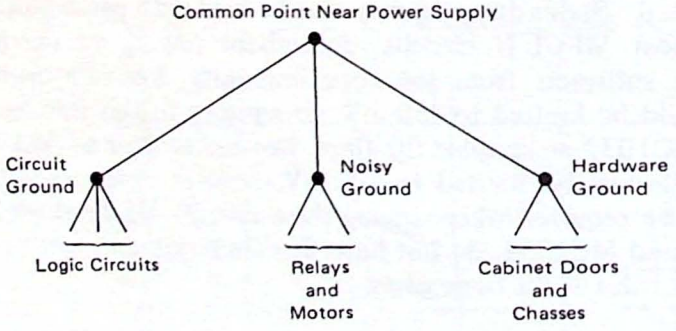
4. For longer signal paths (e.g. between panels or between cabinets) twisted pair lines are recommended. The twisted pair is connected to the OR and NOR outputs at the sending end and to an MC1020 line receiver at the receiving end. With this technique, long lines (hundreds of feet) have been driven with no system degradation other than propagation delay down the line.

E. *System Considerations*

1. A good system ground is required for best performance. All grounds should be connected to a common ground point – normally near the power supply. All logic circuits are connected to a circuit ground. All relays, solenoids, motors and other noise generating devices are wired to a separate ground network connected to the common ground point. Standard noise suppression techniques should be employed (i.e. diodes across relays, and capacitors across dc motor brushes).

All mechanical parts such as panels, chassis, and cabinet doors should be grounded with a third ground. A mounting frame is often used for this if good conduction can be made at points of contact. If some pieces of equipment in the system are left ungrounded they may carry transient voltages that will interfere with the rest of the system. The three separate ground systems connected to a common

2-10: Grounding System



point will eliminate noise on the signal ground (cf Figure 2-10). Heavy ground leads should be used on large systems to minimize any voltage drop along the ground line run.

2. Twisted pair lines and line receivers are normally used between sections of a system unless line lengths can be kept short. Twisted pair lines should always be used between sections operating at widely differing temperatures (>40°C), or between sections not connected with a solid ground network.

2. MECL 10,000 Design Rules

The MECL 10,000 family is a high speed (2 ns propagation delay), economical logic family designed to fill the gap between the MECL II (4 ns) and MECL III (1 ns) families and to meet the requirements for future high performance systems. The family is designed to drive terminated transmission lines with impedances as low as 50 ohms. Also, increased circuit complexity is possible due to high component densities and very low speed-power products. Finally, the relatively slow edge speeds of MECL 10,000 minimize wiring constraints on a logic system.

This section contains layout and design guidelines for power distribution, ground planes, terminations, line lengths, fanout loading, clock distribution, thermal considerations, and packaging, applicable to MECL 10,000.

A. *General Considerations*

1. Standard double-sided plated-through-hole printed circuit boards may be used with the MECL 10,000 family. However multilayer boards will permit a higher component density for a given board area. As a result interconnect lengths are reduced, making the highest speed systems possible.

2. Backplane wire wrapping is also acceptable using commercially available boards. Rules and techniques will be discussed for interconnection lengths and terminations as a function of loading.

3. Coaxial cable, ribbon cable, or twisted pair line is normally required to interface between drawers and card racks in a large system. Microstrip lines are normally required for clock distribution with either series or parallel termination. Series damping resistors can be used to facilitate driving long, unterminated lines.

B. *Printed Circuit Card Layout Techniques*

1. For double-sided boards, a ground plane is recommended on one side of the card. This plane provides a stable ground reference for microstrip transmission lines on the other side of the board. Such transmission lines will have a characteristic impedance of less than 150 ohms. If a ground plane is not possible, a ground bus must be used as part of the layout on the board, to provide a low inductance V_{CC} line.

2. If possible, run the interconnections on one side of the board in the direction perpendicular to the interconnections on the other side of the board. (This works nicely for large boards holding 100 or more packages).

3. The ground plane or bus should be connected to 10% of the edge connector pins spaced equally apart. This reduces the ground impedance, in turn minimizing crosstalk – since multiple signals do not have to rely on a single ground return path.

4. The V_{CC1} and V_{CC2} package pins should be connected directly to the ground plane or bus, as close to the package as possible. Having the two V_{CC} pins and connecting the collectors of emitter follower outputs to only one V_{CC} pin is designed to minimize internal crosstalk.

5. The ground for high current devices – relays, lamps, core drivers, etc. – should be separate from the logic ground. These high current circuits should be connected to a separate ground bus on the card and in the backplane. The separated grounds should be connected at the system ground point.

6. Signal interconnection wires between circuits should be kept as short as possible.

C. *Power Supply Bypassing on Circuit Cards*

1. A 1.0 μF bypass capacitor is used on each board at the power supply inputs. Decouple every 4 to 5 packages with 0.01 μF to 0.1 μF RF quality capacitors (-5.2 Vdc to ground).

2. The power supply ground line noise should be limited to less than 50 mV peak-to-peak.

3. Maintain V_{EE} power supply voltage with less than 100 mV difference among all the logic cards to which signals must interconnect. (This will limit noise margin degradation to less than 30 mV).

4. Power supply regulation should be better than ±10%.

D. *Backplane and Loading Considerations*

1. Wire wrapping techniques are acceptable in the backplane as long as the interconnection rules are followed.

2. A ground screen or ground plane is recommended in the backplane. This gives backplane wiring a characteristic impedance of approximately 140 ohms. (This may vary as much as ±50% depending on distance from the plane and the route taken). The capacitance of the wire over the ground screen is about 1 pF/in and the inductance is about 20 nH/in. Parallel terminating resistors, as described in Chapters 3 and 7, may be used to increase line lengths in the backplane.

3. 10% of the card edge connector pins should be connected to the ground plane or screen to reduce card-to-backplane ground impedance. The lowered ground impedance resulting from many pins paralleled to ground minimizes crosstalk since several signals do not have to rely on a single ground return path.

4. The optimum choice for backplane wiring (for maximum line impedance continuity) is the strip line motherboard technique. In such a case, board interconnections on the motherboard would follow the same rules as the strip line circuit card. Strip line techniques will be discussed in later sections (Chapter 3 and Chapter 7).

5. Series damping resistors can be used to series terminate the interconnect wires as follows:

a. Ten inches of open wire (with a 600 Ω output emitter pulldown resistor connecting to -5.2 volts) can be driven if a 50 ohm resistor is placed in series at the sending end. Up to eight loads may be driven using this configuration. Eighteen inches of line with up to 4 loads may be driven by using a 100 ohm series resistor. These resistor values will insure that any undershoot will be less than 100 mV.

b. Ten inches of open wire may be driven in series with 10 inches of printed circuit line (in either order) if a 100 ohm resistor is placed in series at the sending end. This arrangement can drive up to 4 loads.

6. Three inches of open wiring with a fanout of up to 4 gate loads will produce less than 100 mV undershoot. A ferrite bead place in the line will increase the open wiring length to 15 inches.

7. A damping resistor or a combination of series/parallel terminations with microstrip lines is required when driving flip-flops whenever fanouts exceed 4 and whenever line lengths are greater than 3 inches.

8. Coaxial cable and twisted pair line are recommended when top speeds and rock-bottom noise pickup is a "must" for signal paths in a backplane. An alternate approach, ample for nearly all requirements, is to use strip lines or microstrip lines in a backplane motherboard as in #4 above.

9. Recommended coaxial cables have characteristic impedances of 50-100 Ω, and time delays of 1.5 ns/ft.

10. Twisted-pair lines may be made of standard hookup wire (AWG 24-28), twisted about 30 turns per foot. Such twisted pair exhibits a characteristic impedance of about 110 ohms.

11. When driving coaxial cables, the printed circuit leads from the driver and receiver (going to the coax) should be kept as short as possible to reduce mismatch reflections, unless microstrip or strip line is used.

12. When driving 110 ohm twisted pair, the pair line should be terminated with a 110 ohm resistor across the differential input to a line receiver (MC10115 or MC10116). A 600 ohm pulldown resistor should be connected to each output of the gate driving the twisted pair.

13. Twenty feet of twisted line can be driven by a MECL 10,000 OR/NOR gate at a frequency of 100 MHz, when received by a line receiver.

14. Twisted pair line is recommended for interconnections whenever a temperature differential of more than 35 °C exists between sections in a system.

15. Twisted pair lines are recommended when high switching-current lines are in close proximity to the proposed signal route or when signals run between drawers or racks. If common mode noise is greater than 1.5 volts, then shielded twisted pair is recommended.

16. Inductance and overshoot are reduced if parallel lines are used to fanout to various loads on different circuit boards in the backplane (this also holds for interconnections on the circuit card). In this way, a parallel fanout of 4 will produce very little more overshoot than a fanout of one.

17. Twisted pair lines should be used to distribute clock signals to different logic boards and drawers in a system.

E. *System Distribution and Grounding*

1. High switching current lines for core drivers, relays, and motors should be separated physically from logic lines. (cf Chapter 4, discussion of crosstalk).

2. Avoid bundled parallel runs as much as possible. Signals in bundled cables produce crosstalk.

3. Signal distribution architecture should minimize wiring delays to permit the highest possible system clock speed. System clock speeds of greater than 40 MHz can be obtained in medium size computers.

4. The ground for the high switching current circuitry, should be separated from the logic ground. All separate grounds should, however, be tied together at one point – the system ground point. In that way, the ground buses will be at the same potential but current cannot be looped since they are connected at only one point.

5. The cabinet should be strapped to the system ground point to make it serve as an electrostatic shield.

6. If the system is in a high noise environment, connect the system ground point to earth ground with a heavy conductor.

7. All the equipment in a system should be grounded.

F. *Loading Rules for MECL 10,000*

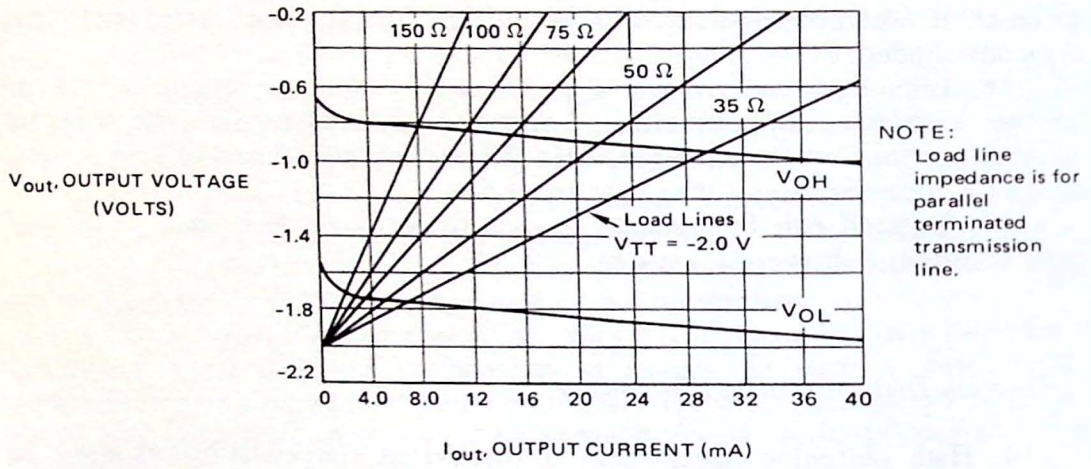
1. A MECL 10,000 gate can drive 25 MECL II gate loads with a 2 kΩ resistor connected from the open emitter output to –5.2 volts.

2. MECL 10,000 and MECL III fanout rules are the same. Minimum output pulldown resistor loading is 50 ohms to -2 volts; 10 gate loads (in addition to the 50 Ω) will reduce noise margin by less than 20 mV. Maximum output pulldown resistor loading is 100 ohms to -2 volts. Larger resistors result in a loss of logic ∅ noise margin. See Figure 2-11 for typical output characteristics of MECL 10,000 as a function of output load current and the value of the output pulldown resistor.

3. It is recommended that output pulldown resistor values of from 270 Ω to 510 Ω (connected to -5.2 V) be used when MECL 10,000 drives MECL 10,000 or MECL III. Under these conditions 25 MECL 10,000 gate loads or 20 MECL III gate loads (50 kΩ Hi-Z input) may be driven.

4. MECL 10,000 fall time is primarily a function of the load capacitance and

2-11: Output Voltage Levels versus DC Loading



the emitter pulldown resistor. If the emitter pulldown is connected to -5.2 V, the fall time is given by:

$$t_f \approx (0.2\ RC + 2)\ ns,$$

where R is the value of the emitter pulldown resistor (in kΩ) and C is the load capacitance (in pF). If the emitter pulldown is connected to -2 V, the fall time is given by:

$$t_f \approx (1.1\ RC + 2)\ ns.$$

5. The propagation delay for the output to go negative is also a function of the load capacitance and the emitter pulldown resistor. If the emitter pulldown resistor is connected to -5.2 V, the propagation delay for the output to go negative is:

$$t_{pd-} \approx (0.1\ RC + 2)\ ns.$$

If the emitter pulldown is connected to -2 V, the formula for the delay is:

$$t_{pd-} \approx (0.47\ RC + 2)\ ns.$$

6. For computing the signal path delay, the typical gate delay for the basic gates is 2.0 ns without capacitive loading. With either a 50 Ω emitter pulldown to -2 volts, or 270 Ω to -5.2 V, propagation delay will increase by 0.1 ns per gate load (assuming 5 pF per gate load).

7. For all MECL 10,000 series devices, the various propagation delays listed in the data sheets have been measured with a 50 ohm emitter pulldown resistor connected to -2 volts. Thus, these propagation delays are longer than would occur for a lighter load condition. Consequently the propagation delays specified on the data sheet are used to determine *maximum* delay paths in a system. (Of course as discussed above, loading will increase the propagation delay and should be allowed for in delay calculations).

8. Emitter dotting is accomplished by tying two or more outputs together. This produces a logic OR function in positive logic. A logic AND function results if negative logic is assigned. For either the 50 Ω or the 270 Ω pulldown, the propagation delay will increase by 50 picoseconds per emitter dot. For loading purposes, each emitter dot may be considered as equivalent to 1/2 a gate load (more precisely, each emitter dot is equivalent to slightly less than 2 pF of capacitive loading).

9. The MECL 10,000 circuit propagation delay is unaffected by the intrinsic line capacitance of an unterminated line. However, overshoot at the receiving end could result in a slightly faster rise time.

10. The MECL 10,000 circuit propagation delay is unaffected by a transmission line properly terminated at the receiving end. Such lines appear as purely resistive loads.

11. High fanout at the end of a terminated transmission line longer than 1.7 ns does not increase the propagation delay of a MECL 10,000 circuit driving the line. Fan-out loading increases the propagation delay of a signal on the line.

12. The delay in signal propagation along a printed circuit line must be taken into consideration. The basic delay of a signal on either a loaded (resistive loading) or unloaded printed circuit surface line over a ground plane is about 1.8 ns per foot or 0.15 ns/in for glass epoxy boards. The exact delay can be calculated using the formula: $t_{pd} = \sqrt{L_o C_o}$, where L_o and C_o are the intrinsic line inductance and capacitance.

13. The signal propagation delay down the line will increase by a factor of $\sqrt{1 + C_d/C_o}$. where C_o is the intrinsic line capacitance and C_d is the capacitance due to loading and stubs off the line:

$$t'_{pd} = t_{pd}\sqrt{1 + C_d/C_o}.$$

14. The increase in signal delay due to load capacitances should be calculated for the particular transmission line characteristics. Lines with low characteristic impedance are less affected because of their higher intrinsic capacitance per unit length.

15. The characteristic impedance of a transmission line is reduced due to load capacitances by the factor $\sqrt{1 + C_d/C_o}$. So, the formula for the modified characteristic impedance, Z'_o, of a transmission line is:

$$Z'_o = \frac{Z_o}{\sqrt{1 + C_d/C_o}},$$

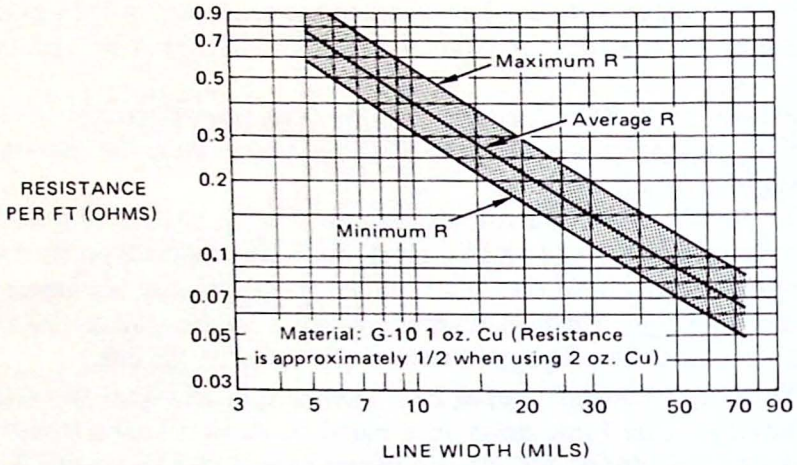
where Z_o is the original line impedance.

16. The maximum line length allowable on the circuit board can be calculated using the data in Figure 2-12 for printed circuit line resistance.

For lines terminated to -2 Vdc at the receiving end of the line, the signal voltage drop in the line is:

$$\Delta V_{Sig} = \left(\frac{2 - |V_{OH}|}{R_T}\right) \cdot (\text{line resistance}),$$

2-12: Resistance versus Line Width for Printed Circuit Lines



where V_{OH} is the logic 1 output voltage and R_T is the terminating resistor. Normally this signal voltage drop is small and need not be calculated. For example, 7 feet of 15-mil wide line will have less than 30 mV drop. The maximum length allowable will be that for which ΔV remains below about 100 mV.

17. The maximum stub length off terminated lines is 3 inches with a fanout of four gate loads on the stub, (for <100 mV undershoot). Whenever an open line (stub) is driven by a pulse, the resultant undershoot and ring are held to about 15% of the logic swing if the two way delay of the line is less than the rise time of the pulse. For these conditions the maximum unterminated line length may be calculated:

$$\ell_{max}\ (\text{in.}) = \frac{t_r}{2t'_{pd}},$$

where t_r is the rise time of the pulse. Here t'_{pd} is the propagation delay of 1 inch of line (cf #13 above).

18. Up to 3 parallel open lines can be driven by one gate, following the rules given above. Parallel fanout to loads is recommended when possible, since lead lengths longer than for a single line may then be used. However, a matched transmission line should be used for driving loads over lines longer than shown in Figure 3-13. Note that both stubs and terminated lines can be driven by one and the same gate.

19. If a ground plane is used, longer lines can be driven than if no ground plane is used; or else the value of a series damping resistor can be reduced. The best approach for determining the permissible values of resistance, length of line, and fanout is from the basic equations that are developed in Chapters 3 and 7.

3. MECL III Design Rules

The MECL III logic family is the fastest standard logic available. This family is designed to fill the high speed (1 ns) requirements of the computer, communication, or instrumentation system designer. MECL III, like MECL 10,000, is designed to drive terminated transmission lines.

Motorola has successfully met the device/package requirements for a 1 ns logic family. The ability to manufacture very fine geometry devices with reliable multilayer metallization results in very compact circuitry and makes LSI possible for MECL; and so, expansion with complex functions operating at higher data rates, lower power, and smaller size than any other form of logic, has become possible with MECL. This is a direct result of new processing technologies and the techniques available to the MECL circuit designer. These techniques include: series gating, collector dotting, and reducing internal logic swing.

The ability to process data with microelectronic structures at bit rates of over 200 million per second requires a thorough understanding of device circuit design, system interconnects, packaging, and thermal management. Specifically, the necessary compromises and possible trade-offs must be understood. A set of layout ground rules or guidelines will provide a first step toward this goal.

A. *Circuit Card Layout*

1. Leave maximum possible spacing among all parallel signal leads to reduce crosstalk. If two signal leads are run parallel at spacings of less than 150 mils, then a ground lead placed between the parallel wires will reduce crosstalk. Such a ground shield will reduce crosstalk from 12 to 7 mV for two 15-mil lines spaced 115 mils with a 35-mil ground shield centered between. If the ground shield is plated through to the ground plane every 1/2", the crosstalk will be reduced even further – to 3 mV.

2. The choice between two-layer and multilayer printed circuit board depends upon the maximum operating frequency and the circuit complexity. With clock rates above 200 MHz, the use of multilayer board is highly recommended. This is due to the possibility of ground loops caused by the use of ground plane areas as signal paths on double layer boards. One to three packages, as in a test fixture, may be used satisfactorily above 200 MHz with two-sided printed circuit board.

B. *Transmission Line (Microstrip Line)*

1. Avoid sharp bends in transmission lines, to prevent reflections from abrupt changes in the characteristic impedance of the line.

2. If two sided board is used, Figure 3-7 may be used to determine Z_o.

3. For MECL systems the physical width of microstrip lines used leads to characteristic impedances usually lying between 50 and 120 ohms. To achieve impedance values greater than 120 ohms, line widths have to be very narrow. This promotes two problems. One is that as dc series resistance goes up, signal level at the receiving end of the line is reduced. The second problem is that "etch-outs" or pin holes exist after etching narrow lines. As a result of various considerations, it happens that 68 ohms is a wise choice of impedance.

An impedance of 68 Ω yields the best trade-off between delay time and power consumption. A 50 Ω line would consume more power. A higher impedance would consume less power, but delay time would increase. As a matter of fact, three impedance levels can serve most applications: 50, 68, and 100 Ω. A 68 ohm stripline is a good choice for on-board uses, while 50 and 100 Ω are used for single ended or party line drive (respectively) off the board.

4. Line characteristic impedance, Z_o, is inversely proportional to the square root of the line capacitance. Therefore, known values of gate input capacitance can be used to modify Z_o, i.e.:

$$Z_o' = \frac{Z_o}{\sqrt{1 + C_d/C_o}} \quad \text{(ohms)},$$

where Z_o' is the new effective characteristic impedance, C_d is the sum of the capacitance due to loads distributed along the line (circuit inputs and stray capacitance), and C_o is the intrinsic line capacitance.

The effect of load capacitances on signal propagation delay time, t_{pd}, is:

$$t_{pd}' = \overbrace{Z_o C_o}^{t_{pd}} \sqrt{1 + \frac{C_d}{C_o}}.$$

If C_d and C_o are in pF, and Z_o in k ohms, t_{pd}' will be in ns.

These relationships show that load capacitances increase propagation delay and will decrease the characteristic impedance. Lines with low characteristic impedance are least affected due to their higher capacitance per unit length.

The one important advantage of transmission lines with proper termination is that stubs have little effect on line delay times. With a Z_o of 50 Ω, stubs must be limited to 1" or less to prevent excessive ringing.

C. *On-Card Clock Distribution Via Transmission Lines*

1. Use of the OR output for gates used as clock buffers is recommended in developing a clock chain or tree. A small clock skew may result from using both the OR and NOR outputs in the chain.

2. Use balanced fanouts on the clock drivers in a tree.

3. Overshoot can be reduced by using two parallel drive lines in place of one

drive line. The effect of this arrangement is to cut the load capacitance per line in half.

4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1 ns.

5. It is always good practice to use a buffer when driving long lines off the card. One instance when a buffer is particularly desireable is when Q or $\overline{Q}$ outputs from a high frequency counter are also used within the feedback logic of the counter.

6. Parallel drive gates are used when high clocking repetition rates are required, and when driving high capacitance loads. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz of bandwidth can be gained with the two (or three) clock driver gates in parallel.

7. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid lumped loads at the end of lines greater than 3 inches long. A lumped load, if used, should consist of no more than four gate loads.

8. For Wired-OR (emitter dotting), two-way lines are required when connection distance is greater than 1 inch. A two-way 100 Ω transmission line is produced by terminating both ends with 100 Ω impedances. Single end termination may be used when all emitter connections are within 1 inch of each other.

D. *Off-Card Clock Distribution*

1. The OR/NOR outputs of an MC1660 may be used to drive into twisted pair lines. At the far end of the twisted pair, an MC1692 differential line receiver is used. The line should be terminated. This may be done with approximately 110 ohms across the differential receiver input.

Alternatively, a 56-ohm resistor from each of the receiver inputs to −2 Vdc will provide both line termination and pulldown resistance for the MC1660 driver. This latter method not only provides high speed board-to-board clock distribution, but also yields noise margin advantages for the system. That is, the noise margin from board-to-board becomes independent of temperature differentials, due to the line receiver operating with differential inputs.

2. MECL III clock distribution to MECL II logic elements can be done in one of two ways:

a) Use the OR/NOR outputs or Q/$\overline{Q}$ outputs to drive twisted pair as above, receiving differentially with the MECL II line receivers. (MC1020, MC1035, or MC1065).

b) Use any MECL III single-rail output to drive MECL II logic, but lightly load the MECL III element (2 kΩ to −5.2 V) and maintain the interface lead length under 1 inch total.

3. MECL III interfaces directly with MECL 10,000. Use the wiring rules for whichever family drives the line.

E. *Testing MECL III*

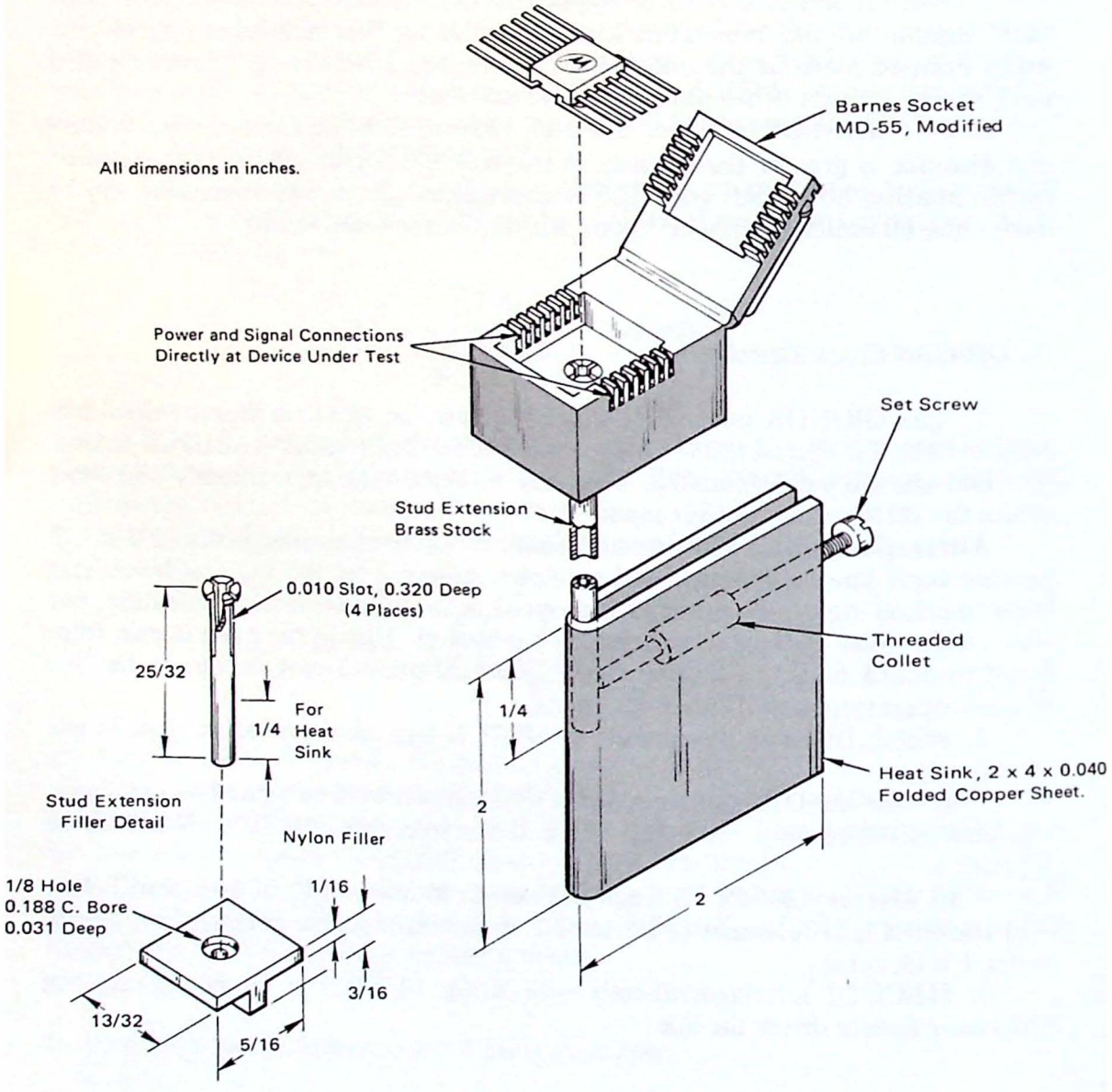
1. Keep all unshielded lead lengths as short as possible, less than 1/4".

2. For stud packages, use a modified Barnes 14-pin flat-pack snap-top socket (or equivalent). Physically cut into the sides of the socket near the upper lead

contacts, so that probe points and power may be connected right at the device under test. (See Figure 2-13).

For dual-in-line packages use AMP 16-pin low profile sockets (or equivalent) which have no long paths from the device under test to the solder pads on the bottom of the socket.

2-13: MECL III Stud Package Test Socket



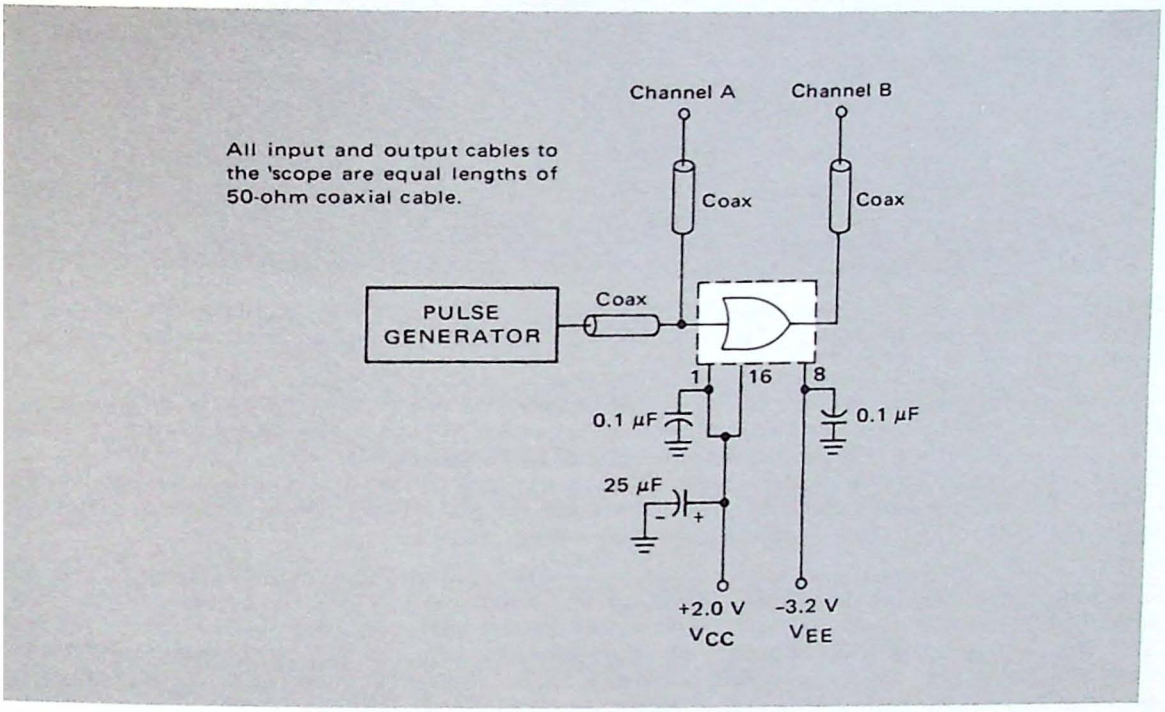
3. Use small RF quality parts: 1/8 W carbon composition resistors and 0.01 μF low inductance disc ceramic capacitors.

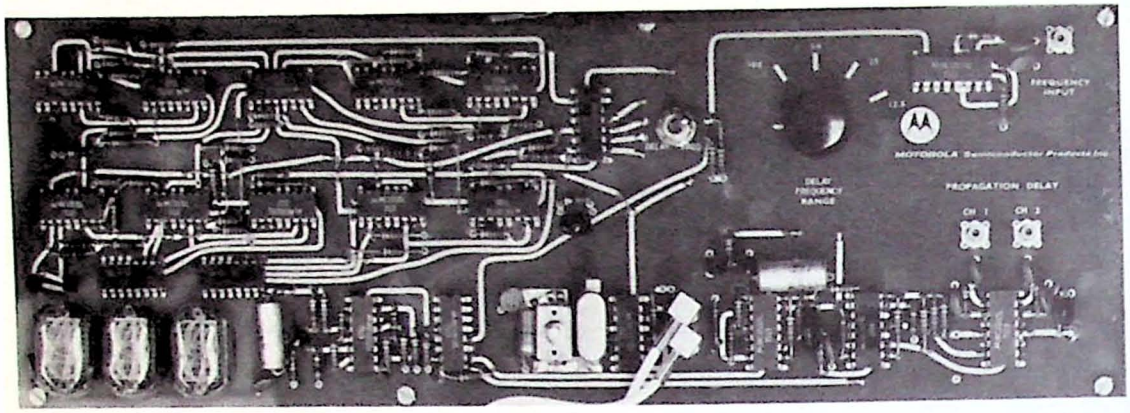
4. All input/output connections should be made with good quality miniature 50 Ω semi-ridge coax, and BNC, GR, or miniature coax fittings.

5. A solid ground plane should be used, with V_{CC} pins 1 and 14 or 16 connected directly to the +2.0 volt plane via the shortest possible path.

6. V_{CC} should be at +2.0 volts with V_{EE} at −3.2 volts. The gate under test should have its output connected to a 3S5/S2-50Ω sampling plug-in for a Tektronix 568 sampling system (or equivalent). The arrangement shown in Figure 2-14 is recommended by Motorola for measuring subnanosecond performance.

2-14: Recommended MECL Test Setup





This demonstration circuit is capable of measuring frequencies in excess of 150 MHz and propagation delays with an accuracy of tenths of a nanosecond. MECL II, MECL III and MECL 10,000 logic functions are used in this circuitry on standard PC board.

For measuring frequency, the standard technique of opening a precision window and counting the input frequency during that interval is used. A 1 μsec window is generated from a 100 MHz crystal oscillator and a counter chain made of MC10131 flip-flops. The sampling rate is determined by a unijunction oscillator. Translation and wave-shaping is accomplished with an MC10115 buffer. This circuitry also provides the reset pulse between sample intervals. The display is used to show the count and is driven by MECL II MC1045 decoder drivers. The most significant digit displays 1 and 0 and is driven by two high voltage transistors.

The propagation delay measurement is more complex since the speed requirements necessitate some form of averaging technique. The two propagation delay inputs are connected to an MC1674 Exclusive NOR gate. The output of this gate gives a pulse duty cycle proportional to the propagation delay between the two signals. MECL III circuits, such as the MC1674, are the only commercially available integrated circuits which can perform this very high speed task – the Exclusive NOR circuit must operate at twice the input frequency. The waveform out of the Exclusive NOR gate is integrated, giving a voltage level proportional to propagation delay. A ramp function is generated and compared to this voltage level. An MC10115 is used as a comparator, outputting a pulse width window, proportional to the propagation delay of the inputs. This window is used to gate the 100 MHz oscillator to the display counter used in frequency measurements.

CHAPTER 3 Printed Circuit Board Connections

Any signal path on a circuit board may be considered a form of transmission line. If the line propagation delay is short with respect to the rise time of the signal, any reflections are masked during the rise time and are not seen as overshoot or ringing. As a result, because of the high ratio of rise time to propagation delay time, signal lines for most MOS circuits may be several feet long without signal distortion. However, as edge speeds increase with faster forms of logic, the line lengths must be shorter in order to retain signal integrity.

Two techniques can be used to enable high speed circuits to operate over relatively long lines without serious waveshape deterioration. TTL uses an input clamp for fast negative edges. The energy of the overshoot is clamped at one diode drop below ground, and this reduces the amplitude of the following undershoot. The slower positive-going edges are allowed to overshoot, but are damped out by the relatively high output impedance (50 to 80 ohms) of the circuit in the logic 1 state. Also, greater noise immunity in the 1 state makes any undershoot less critical.

The disadvantages of the TTL technique show up at higher bit rates and faster edge speeds when fanouts along the line are used. Since the reflections are present in the lines, they will tend to combine at high bit rates to cause signal distortions and loss of noise immunity.

Consequently, MECL uses another approach for handling reflection problems: matching the impedance of the line. In this way, reflections are controlled and signal integrity is maintained.

This chapter discusses circuit interconnections as transmission lines, with the open line treated as an unterminated line. Although MECL III is the only family with a strict requirement for a transmission line environment, it is expected that most MECL 10,000 users will use matched impedance lines to improve interconnection distances and signal purity.

Circuit designers have a choice between transmission lines and conventional interconnect wiring when the distances between MECL devices are short, less than the lengths in Figure 1-7, #16 or when the rise times are greater than 3 ns. The design decision must be made after thorough analysis of the system requirements. Incorrect selection of conventional interconnect wiring could result in false system operation due to a high percentage of incident pulse reflections and subsequent lowering of the ac noise immunity.

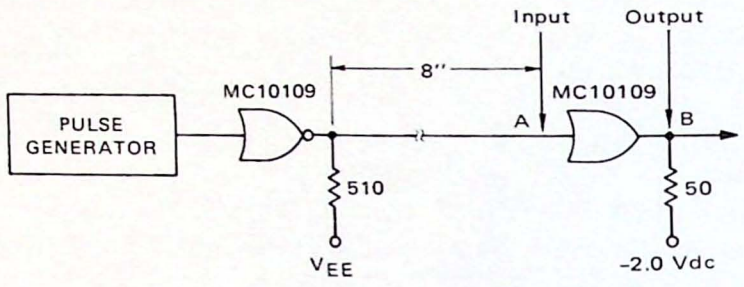
In many cases where MECL devices are used, transmission line techniques are advantageous. When using MECL devices with rise times less than 3 ns, transmission lines are highly recommended. The basic factors which will affect this decision are:

A. System rise time
B. Interconnect distance
C. Capacitive loading (fanout)
D. Resistive loading (line termination)
E. Percentage of undershoot and overshoot permissible (reduction in ac noise immunity).

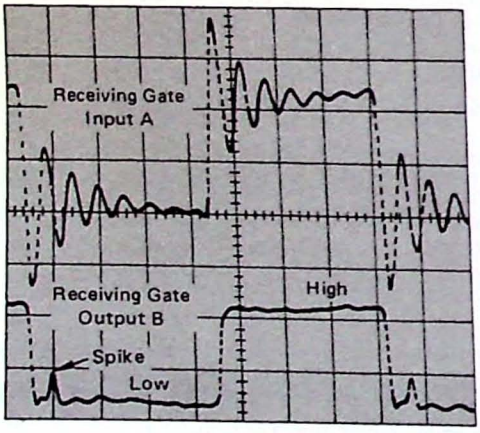
The result of analyses shows that transmission lines should be used if the percentages (E, above) exceed the acceptable design goal. A general rule of thumb that can be used is that undershoot should not exceed 10%, and overshoot should not exceed 35% of the logic swing. The 35% overshoot limit keeps the input out of saturation and the 10% undershoot is less than 100 mV loss of noise margin. Actually, most MECL circuits can tolerate up to 30% undershoot.

An example of a MECL 10,000 device driving an 8-inch open wire is shown in Figure 3-1. The oscilloscope traces, for the 8-inch open wire without a ground plane,

3-1: Overshoot and Undershoot With an Open Wire Line



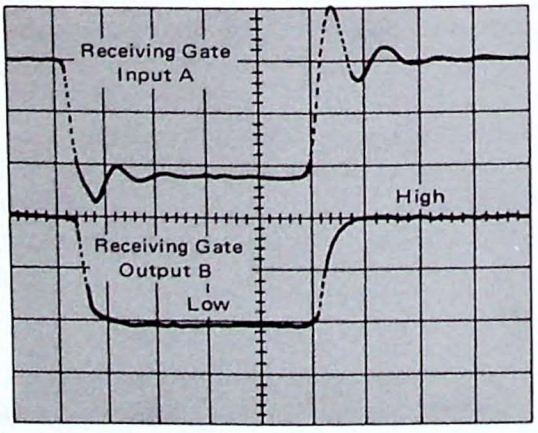
(a) Test Arrangement



(b) Ground Plane Not Used

Vertical Scale = 400 mV/cm
Horizontal Scale = 20 ns/cm

(c) Ground Plane Added



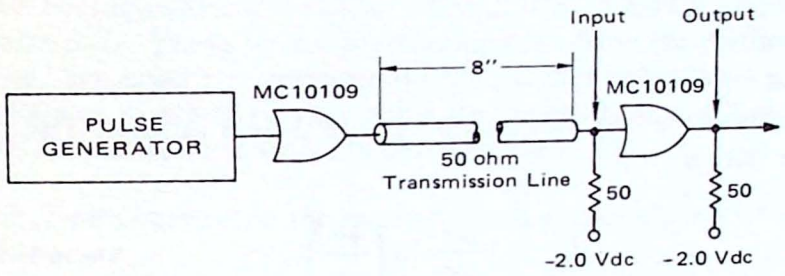
Vertical Scale = 400 mV/cm
Horizontal Scale = 10 ns/cm

taken at points A and B are shown in Figure 3-1 (b). Trace A shows an overshoot condition of 60% and an undershoot of 40%. It can be seen how this undershoot condition affects trace B during the low level period of the signal – a small spike is produced.

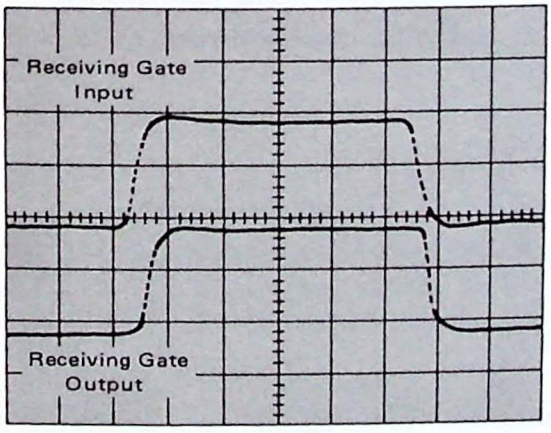
By way of contrast to the open wire circuit, a ground plane is added and the trace shown in Figure 3-1(c) is obtained. The addition of a plane reduces overshoot and undershoot to about 40% and 20% respectively.

Figure 3-2(a) shows an 8-inch transmission line correctly terminated. The scope traces in Figure 3-2(b) indicate the marked advantages of using transmission lines correctly terminated.

3-2: Matched Transmission Line Waveshapes



(a) Test Configuration



Vertical Scale = 400 mV/cm
Horizontal Scale = 10 ns/cm

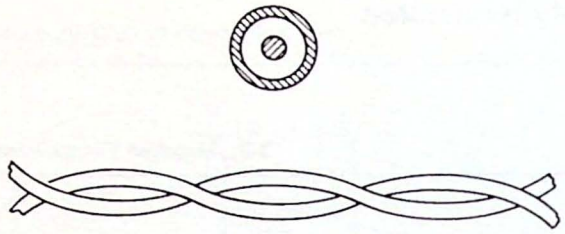
(b) Input and Output Waveforms

Transmission Line Geometries

Figures 3-3 through 3-6 show some of the types of transmission lines than can be used for interconnecting high speed logic systems. Details concerning each type are elaborated in the following paragraphs.

Coaxial Cable and Twisted Pair

Figure 3-3 shows a twisted pair line and the cross section of a coaxial cable transmission line. Some common types of coaxial cable have characteristic impedances of 50, 75, 93, or 125 ohms. Twisted pairs can be made from standard hook-up wire (AWG 24-28) twisted about 30 turns per foot. Such twisted pair has a characteristic impedance of about 110 ohms. Coaxial cable and twisted pair are recommended for long line lengths in the backplane.



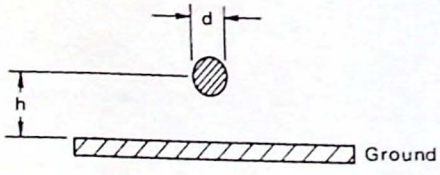
3-3: Coaxial Cable, Twisted Pair

Wire Over Ground

Figure 3-4 shows the cross section of a wire over a ground. The characteristic impedance of the wire is

$$Z_o = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4h}{d}\right),$$

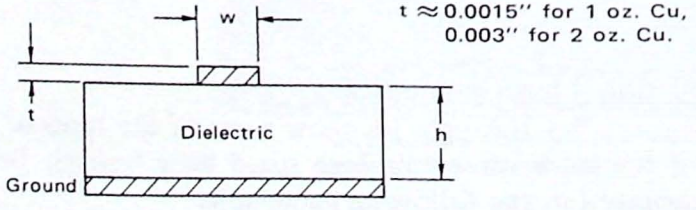
where e_r is the effective dielectric constant surrounding the wire. The wire over a ground plane is most useful for breadboard layout and for backplane wiring. The characteristic impedance of a wire over a ground plane in the backplane is about 120 ohms, although this may vary as much as ±40% depending on the distance from the plane, proximity of adjacent wires, and the configuration of the ground.



3-4: Wire Over Ground

Microstrip Lines

A microstrip line (Figure 3-5) is a strip conductor (signal line) separated from a ground plane by a dielectric. If the thickness, width of the line, and the distance



3-5: Microstrip

from the ground plane are controlled, the line will exhibit a predictable characteristic impedance that can be controlled to within ±5%.

The characteristic impedance, Z_o, of a microstrip line is:

$$Z_o = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right),$$

where:

e_r = relative dielectric constant of the board material (about 5 for G-10 fiber-glass epoxy boards),
w, h, t, = dimensions indicated in Figure 3-5.

The signal line is made by etching away the unwanted copper using photo resist techniques. The characteristic impedance of microstrip lines for various geometries is plotted in Figure 3-7. These values were calculated from the mathematical relation above and closely agree with experimental time domain reflectometer measurements. In fact, the equation proves to be very accurate for ratios of width to height between 0.1 and 3.0 and for dielectric constants between 1 and 15.

Figure 3-8 shows curves for the microstrip capacitance per foot as a function of line width and spacing.

The inductance per foot may be calculated using the formula:

$$L_o = Z_o^2 C_o,$$

where: Z_o = characteristic impedance,

C_o = capacitance/ft.

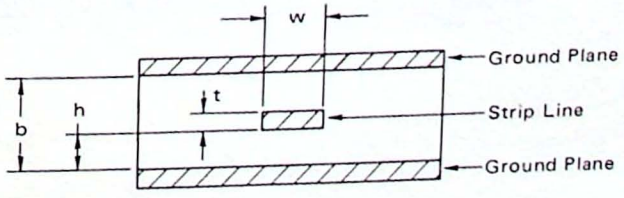
The propagation delay of the line may be calculated by:

$$t_{pd} = 1.017 \sqrt{0.475\, e_r + 0.67} \quad \text{ns/ft}.$$

Note that the propagation delay of the line is dependent only on the dielectric constant and is not a function of line width or spacing. For G-10 fiber-glass epoxy boards ($e_r \cong 5.0$) the propagation delay of the microstrip line is calculated to be 1.77 ns/ft.

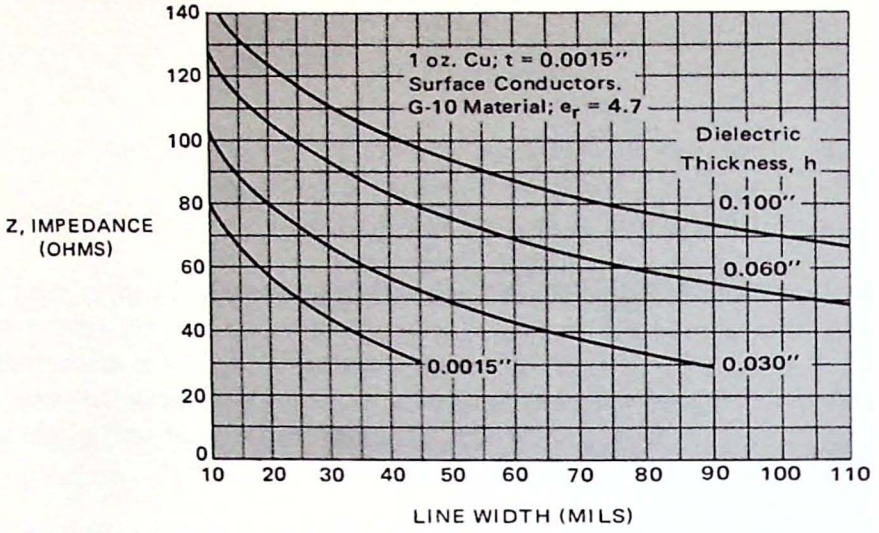
Strip Line

A strip line (Figure 3-6) consists of a copper ribbon centered in a dielectric medium between two conducting planes. If the thickness and width of the line, the

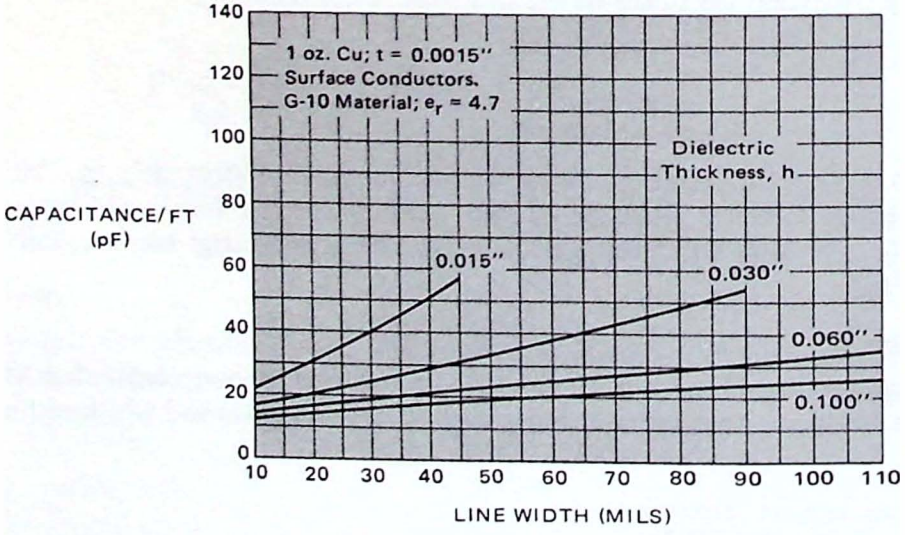


3-6: Stripline

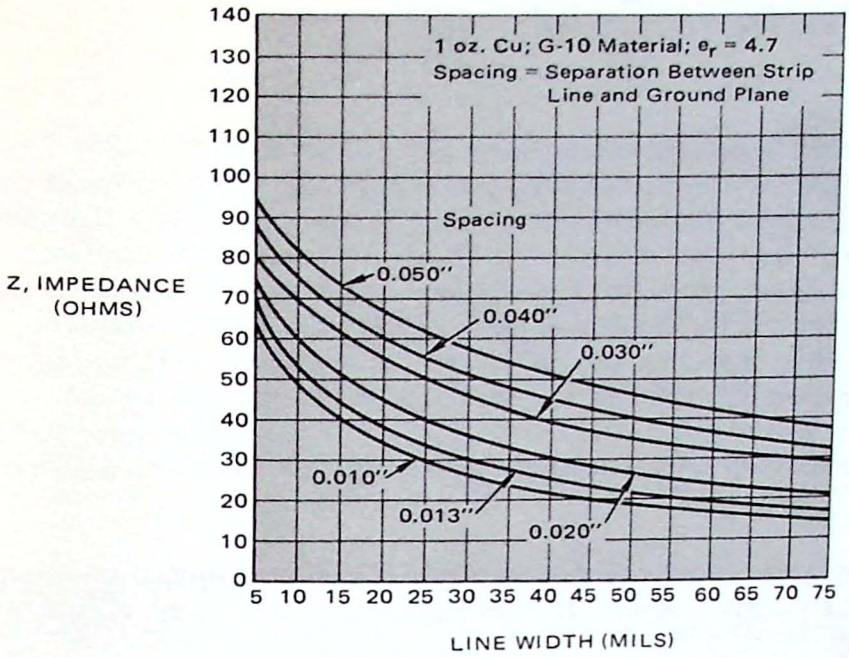
3-7: Impedance versus Line Width and Dielectric Thickness for Microstrip Lines



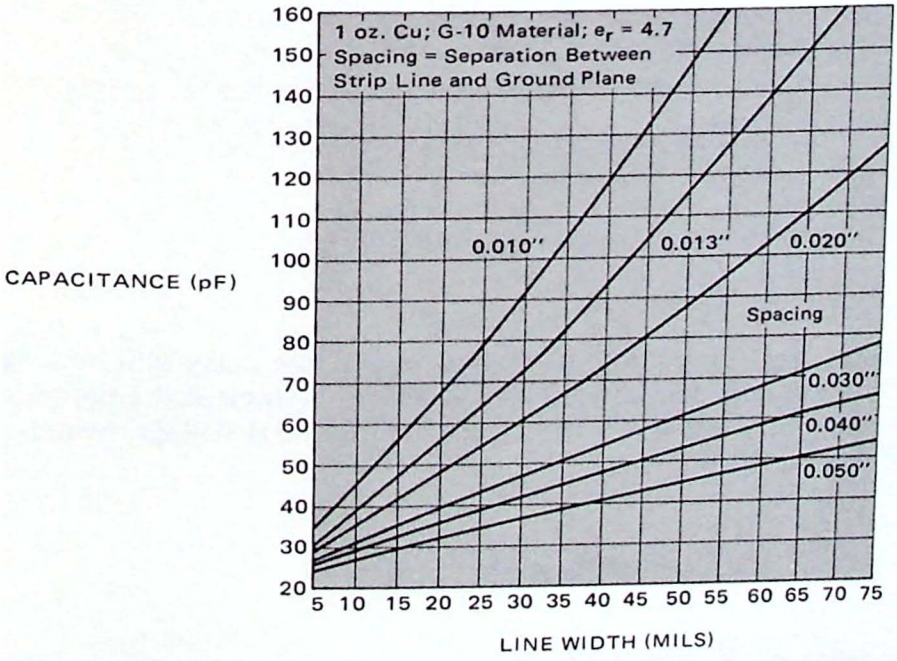
3-8: Capacitance versus Line Width and Dielectric Thickness for Microstrip Lines



3-9: Impedance versus Wire Width and Spacing for Strip Lines



3-10: Capacitance versus Line Width and Spacing for Strip Lines



dielectric constant of the medium, and the distance between the ground planes are all controlled, the line will exhibit a characteristic impedance that can be held constant within ±5%. The characteristic impedance of a strip line is theoretically:

$$Z_o = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4b}{0.67\,\pi w(0.8+\frac{t}{w})}\right).$$

This equation proves accurate enough for $w/(b-t)<0.35$ and $t/b<0.25$.

Figure 3-9 gives the actual characteristic impedance for various geometries of stripline. These values were measured with a time domain reflectometer. The measured results closely parallel those calculated from the above equation.

Figure 3-10 shows curves for the stripline capacitance per foot for various line widths and spacings. An LC meter was used to determine the capacitance.

The inductance per foot can be calculated using the relation $L_o = Z_o^2 C_o$, while the propagation delay of the line can be found from the relation:

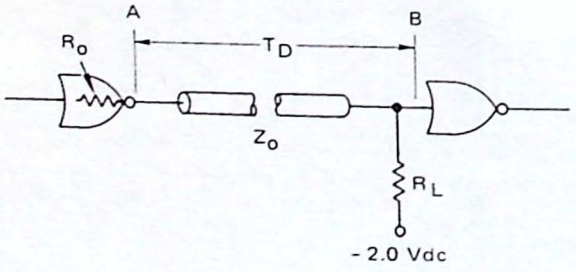
$$t_{pd} = 1.017\sqrt{e_r} \quad \text{ns/ft}.$$

For G-10 fiber-glass epoxy boards ($e_r \cong 5.0$), the propagation delay of the strip lines is 2.26 ns/ft. Again, the propagation delay is not a function of line width or spacing.

Basic Transmission Line Operation

The behavior of signals on a transmission line is important for understanding the methods used to terminate MECL lines. Figure 3-11 shows a line with typical

3-11: MECL Transmission Line



loads at both ends. For the purpose of discussion the line delay will be long with respect to the rise time so that reflections will appear at their full amplitude. The output voltage swing at point A is a function of the internal voltage swing, output impedance, and line impedance:

$$\Delta V_A = \Delta V_{INT}\left(\frac{Z_o}{R_o + Z_o}\right).$$

Since R_o is small compared to line impedance, the output swing is nearly the same as the input transition. The internal voltage swing is approximately 900 mV, giving a typical output swing greater than 800 mV.

This signal propagates down the line and is seen at point B time T_D later. The voltage reflection coefficient at the load end of the line, ρ_L, is a function of the line characteristic impedance and the load impedance:

$$\rho_L = \frac{R_L - Z_o}{R_L + Z_o} .$$

Clearly, for the ideal case of $R_L = Z_o$, there is no reflection. More important, for any value of R_L close to Z_o the reflection is quite small. At time 2 T_D any reflection returns to point A and is again reflected, by the sending end reflection coefficient ρ_S:

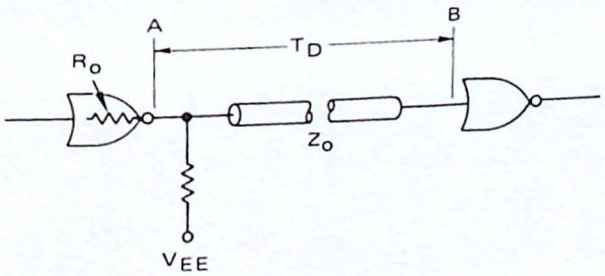
$$\rho_S = \frac{R_o - Z_o}{R_o + Z_o} .$$

The reflection continues bouncing back and forth between the ends of the line, being successively reduced by the reflection coefficients and the resistance in the line.

Unterminated Lines

Figure 3-12 shows a specific transmission line variously known as an "open line," an "unterminated line" or a "stub." Behavior of this line is as follows. At time zero an initial, full MECL signal starts at point A. Time T_D later the signal reaches point B and is reflected by ρ_L discussed previously. Since the input impedance of the driven gate is very high with respect to Z_o, a large positive reflection occurs and signal overshoot results. At time 2 T_D the reflection is back at point A and is reflected by ρ_S. Because of the low value of R_o the reflection is in the negative direction (refer to equation for ρ_S), resulting in a signal at point B at time 3 T_D that is in the opposite direction to the initial signal. This signal at B at 3 T_D and its subsequent reflections produce the undershoot which subtracts from signal noise immunity. These reflections, successively smaller, cause the condition known as "ringing " as shown in Figure 3-1(b).

3-12: MECL Unterminated Transmission Line



If the lines are sufficiently short, the signal still will be rising at time T_D, and reflections are part of the rising edge. With longer lines, the rise of the signal will be completed before a time T_D, and reflections will appear as overshoot and

undershoot. For this reason, unterminated or undamped lines have maximum recommended lengths when used with MECL logic.

The undershoot caused by an unterminated line is held to about 15% of the logic swing if the two way delay of the line is less than the rise time of the pulse. The maximum open line length may be calculated by expressing this rule with the relation:

$$\ell_{max} \leqq \frac{t_r}{2t_{pd}} ,$$

where: t_r = rise time,

t_{pd} = propagation delay of the line per unit length.

(Use t'_{pd} when line is loaded, cf equation 11, Chapter 7).

It can be seen that the slower rise times of MECL II and MECL 10,000 are compatible with open lines, but that line lengths are important for the faster MECL III. The other variable for line length, t_{pd}, is controlled by the type of line (velocity factor) and the loading on the line. Increased loading raises the propagation delay and accounts for the decreasing permissible line length with increasing fanout (cf Figure 2-7). The analysis of rate of propagation with line loading is covered in Chapter 7.

Suggested maximum open line lengths for MECL 10,000, high speed MECL II (i.e. MECL II-1/2) and MECL III are tabulated in Figures 3-13, 3-14, and 3-15 for

3-13: Maximum Open Line Length for MECL 10,000 (Gate Rise Time = 3.5 ns)

	Z_o (OHMS)	FANOUT = 1 (2.9 pF)	FANOUT = 2 (5.8 pF)	FANOUT = 4 (11.6 pF)	FANOUT = 8 (23.2 pF)
		ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX (IN)
MICROSTRIP (Propagation Delay 0.148 ns/in.)	50	8.3	7.5	6.7	5.7
	68	7.0	6.2	5.0	4.0
	75	6.9	5.9	4.6	3.6
	82	6.6	5.7	4.2	3.3
	90	6.5	5.4	3.9	3.0
	100	6.3	5.1	3.6	2.6
STRIPLINE (Propagation Delay 0.188 ns/in.)	50	6.5	5.9	5.2	4.5
	68	5.6	4.9	3.9	3.2
	75	5.3	4.7	3.6	2.8
	82	5.2	4.4	3.3	2.6
	90	5.1	4.3	3.1	2.4
	100	4.9	4.0	2.8	2.1
BACKPLANE (Propagation Delay 0.140 ns/in.)	100	6.6	5.4	3.8	2.8
	140	5.9	4.3	2.8	1.9
	180	5.2	3.6	2.1	1.3

3-14: Maximum Open Line Length for High Speed MECL II (Gate Rise Time = 2 ns)

	Z_o (OHMS)	FANOUT = 1 (3.3 pF)	FANOUT = 2 (6.6 pF)	FANOUT = 4 (13.2 pF)	FANOUT = 8 (26.4 pF)
		ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX(IN)	ℓ MAX (IN)
MICROSTRIP (Propagation Delay 0.148 ns/in.)	50	3.5	2.8	1.9	1.2
	68	3.2	2.3	1.5	0.8
	75	3.0	2.2	1.3	0.7
	82	2.9	2.0	1.2	0.6
	90	2.8	1.9	1.0	0.5
	100	2.6	1.8	0.9	0.4
STRIPLINE (Propagation Delay 0.188 ns/in.)	50	2.8	2.2	1.5	1.0
	68	2.5	1.9	1.2	0.6
	75	2.4	1.7	1.1	0.6
	82	2.3	1.6	0.9	0.5
	90	2.2	1.5	0.8	0.4
	100	2.0	1.4	0.7	0.3
BACKPLANE (Propagation Delay 0.140 ns/in.)	100	2.8	1.8	0.9	0.4
	140	2.4	1.4	0.5	0.3
	180	2.0	1.0	0.3	0.1

3-15: Maximum Open Line Length for MECL III (Gate Rise Time 1.1 ns)

	Z_o (OHMS)	FANOUT = 1 (3.3 pF)	FANOUT = 2 (6.6 pF)	FANOUT = 4 (13.2 pF)	FANOUT = 8 (26.4 pF)
		ℓ (MAX (IN)	ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX (IN)
MICROSTRIP (Propagation Delay 0.148 ns/in.)	50	1.6	1.1	0.7	0.6
	68	1.4	0.8	0.5	0.4
	75	1.3	0.8	0.4	0.3
	82	1.2	0.7	0.4	0.2
	90	1.1	0.6	0.3	0.2
	100	1.0	0.5	0.2	0.1
STRIPLINE (Propagation Delay 0.188 ns/in.)	50	1.2	0.8	0.6	0.5
	68	1.1	0.7	0.4	0.3
	75	1.0	0.6	0.3	0.2
	82	0.9	0.6	0.3	0.2
	90	0.9	0.5	0.2	0.1
	100	0.8	0.4	0.2	0.1
BACKPLANE (Propagation Delay 0.140 ns/in.)	100	1.1	0.6	0.2	0.1
	140	0.8	0.3	0	0
	180	0.6	0.2	0	0

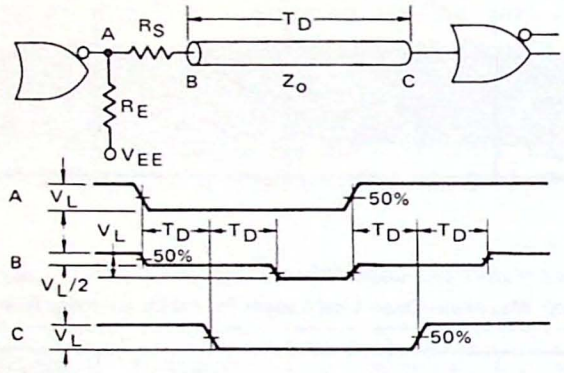
various fanouts and line impedances. For these tables, line lengths are chosen to limit overshoot to 35% of logic swing and undershoot to 12%.

Series Damped and Series Terminated Lines

Overshoot and ringing on longer lines may be controlled by using series damping or series terminating techniques. Series damping is accomplished by inserting a small resistor (typically 10-75Ω) in series with the output of the gate as shown in Figure 3-16. This technique can be used with all MECL families and is associated with lines not defined by a controlled characteristic impedance, (e.g. back-plane wiring, circuit boards without ground plane, and most wire wrapped connections).

The series termination is a specialized case of damping in which the resistor value plus the circuit output impedance is equal to the impedance of the transmission line. The waveforms in Figure 3-16 and the following description of operation are for series termination. A similar analysis may be done for any value of damping resistor and line impedance.

3-16: Driving a Series Terminated Line



The impedance looking back toward the driving gate at point B should be equal to the characteristic impedance of the transmission line. The dc output impedance is 5 ohms for a MECL III gate and 7 ohms for a MECL 10,000 gate. AC output impedance is only slightly higher than the dc impedance values. Therefore, if Z_o is 75 ohms, then the value of R_S must be approximately 68 ohms.

At time = 0, the internal voltage in the circuit switches to the low state which represents a change of 0.9 volts (ΔV_{INT} = -0.9 V). The voltage change at point B can be expressed as:

$$\Delta V_B = \Delta V_{INT}\left(\frac{Z_o}{R_S + R_o + Z_o}\right) ,$$

where R_o is the output impedance of the MECL gate.

Since $R_S + R_o$ is made equal to Z_o for a series terminated line, then the voltage change at B is 1/2 the voltage, ΔV_{INT}. It takes the propagation delay time

of the transmission line, T_D, for the waveform to reach point C, where the voltage doubles due to the near unity reflection coefficient at the end of the line. The reflected voltage, which is equal to the sending voltage, arrives at point B at a time, T_D, later. No more reflections occur if $R_S + R_O$ is equal to Z_O. Similar waveforms occur when the driving gate switches from the low to the high state.

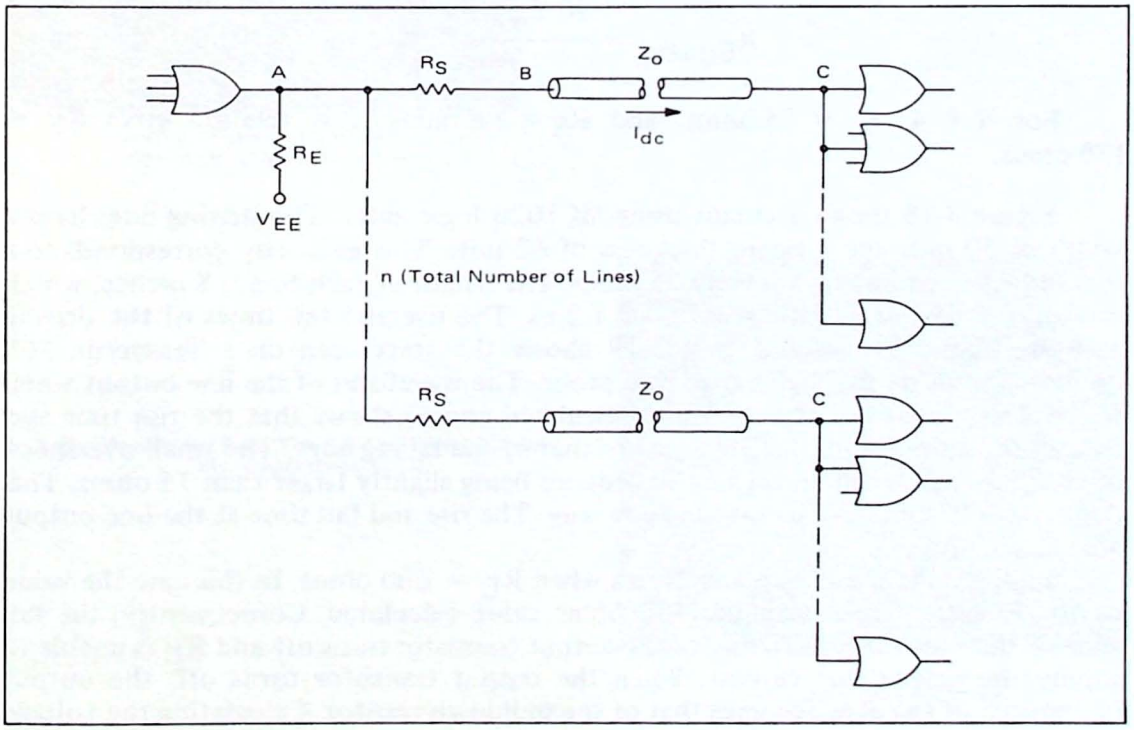
One of the advantages of using series terminated lines is that only the logic power supply is required. Another advantage is the lower overall power requirements. One power supply can also be used with parallel terminated lines described in the next section, but two resistors must be used for the total termination resistor, resulting in the need for considerably more power. In addition, when two power supplies are used with parallel terminated lines using one termination resistor, an extra voltage bus or plane is required to supply -2.0 volts to the termination resistors.

A disadvantage of series termination is that distributed loading along the line cannot be used, because of the half-voltage waveform travelling down the line (see Figure 3-16, waveform B). However there is no limit on the number of lumped loads that can be placed at the end of the series terminated line imposed by reflections at the receiving gate, since all the reflections will be absorbed at the source. Nevertheless, voltage drop across the series terminating resistor due to input current, limits loading to less than 10.

The distance permitted among the receiving gates at the end of the line can be found from Figures 3-13, 3-14, or 3-15. For example, if MECL III were used with 50 ohm microstrip lines, the maximum total separation of four gate loads at the end of a series terminated line is 0.7 inches (see Figure 3-15).

The disadvantages of slower propagation delay and using only lumped loading at the end of a series terminated line can be eliminated at the expense of more transmission lines, as in Figure 3-17. For parallel fanout, n transmission lines can be

3-17: Parallel Fanout Using Series Termination



used. The value chosen for R_S should be the same as discussed previously when n was equal to one.

To determine the value of the emitter pulldown resistor, R_E, the following procedure is recommended.

The value of R_E must be small enough to supply each transmission line with the necessary current. If R_E is made too large, the output transistor will turn off when switching from the high to the low voltage state. The maximum value for R_E can be derived by equating the voltage point at which the output transistor turns off with the midpoint of the logic swing:

$$\Delta V_B = \Delta V_{INT} \left(\frac{Z_o}{R_S + R_o + Z_o} \right) ,$$

where: ΔV_B = one half the logic swing = 400 mV,

ΔV_{INT} = V_{EE} - logic 1 level = (5.2 - 0.8) V = 4,400 mV, (since the output transistor is turned off, it does not affect the calculation),

R_S = series damping resistance,

R_o = R_E (because the output transistor is turned off).

So:

$$R_{E(max)} = 10 Z_o - R_S .$$

Finally, when n parallel lines are driven as in Figure 3-17:

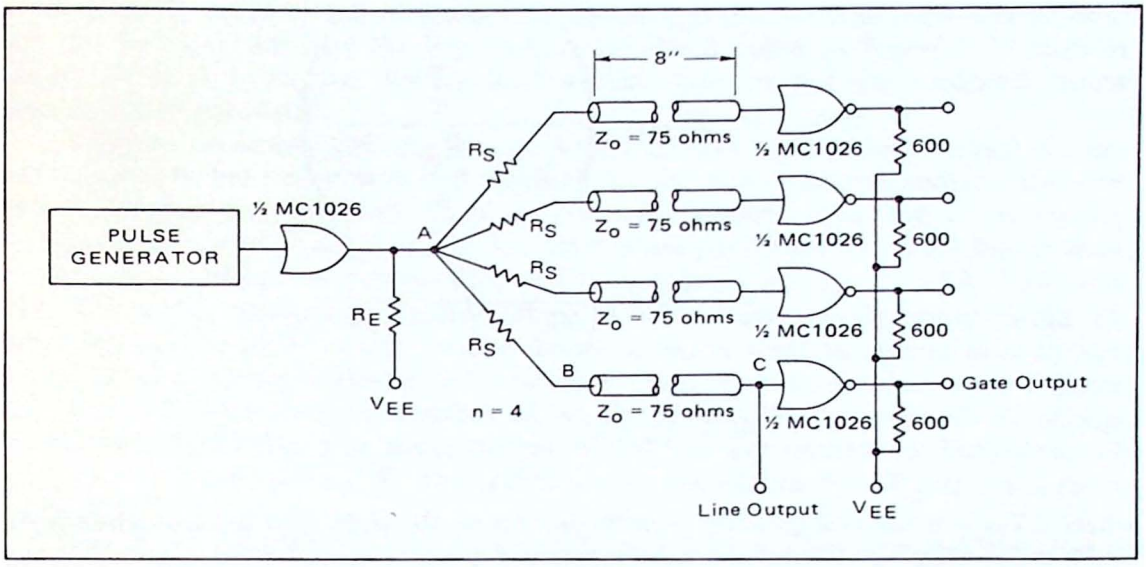
$$R_{E(max)} = \frac{10 Z_o - R_S}{n} .$$

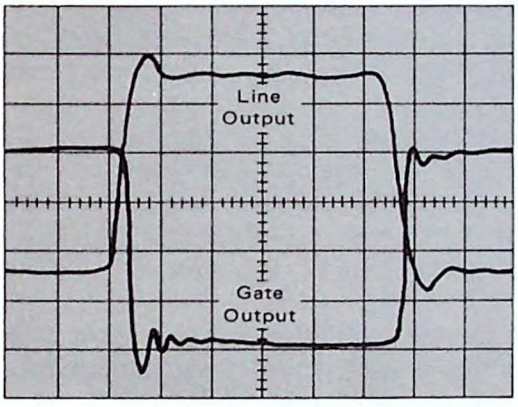
For n = 4, Z_o = 75 ohms, and R_S = 68 ohms, this relation gives R_E = 170 ohms.

Figure 3-18 shows a circuit using MC1026 logic gates. The driving lines have a width of 50 mils and a board thickness of 62 mils. This geometry corresponds to a line impedance of approximately 75 ohms. The length of each line is 8 inches, which produces a line propagation delay of 1.2 ns. The rise and fall times of the driving gate are about 2 ns each. Figure 3-19 shows the trace seen on a Tektronix 567 oscilloscope using the high impedance probe. The waveform of the line output when R_E = 180 ohms (close to the value calculated above) shows that the rise time and overshoot of the rising edge are equal to that of the falling edge. The small overshoot of about 50 mV is due to the line impedance being slightly larger than 75 ohms. This does not affect circuit operation in any way. The rise and fall time at the line output are each 3.3 ns.

Figure 3-20 shows the waveforms when R_E = 600 ohms. In this case the value of R_E is much larger than the 170 ohms value calculated. Consequently, the fall time of the waveform suffers since the output transistor turns off and R_E is unable to supply the proper line current. When the output transistor turns off, the output impedance of the gate becomes that of the pulldown resistor. Calculating the voltage

3-18: Series Termination Test Set-Up Using the MC1026 Gates

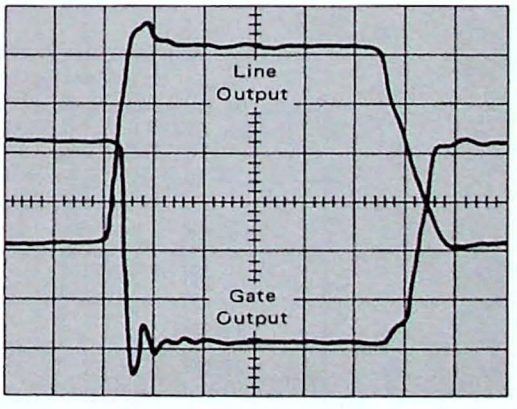




Vertical Scale = 0.2 V/cm
Horizontal Scale = 10 ns/cm

3-19: Waveforms from Test Set-Up of Figure 3-18
(R_E = 180 ohms, n = 4)

3-20: Waveforms from Test Set-Up of Figure 3-18
(R_E = 600 ohms, n = 4)



Vertical Scale = 0.2 V/cm
Horizontal Scale = 10 ns/cm

change at point B shows a ΔV of:

$$\Delta V_B = \Delta V_{INT} \left(\frac{\frac{Z_o}{n}}{R_E + \frac{R_S}{n} + \frac{Z_o}{n}} \right)$$

$$= (-4{,}400) \left(\frac{19}{600 + 17 + 19} \right)$$

$$\approx -130 \text{ mV},$$

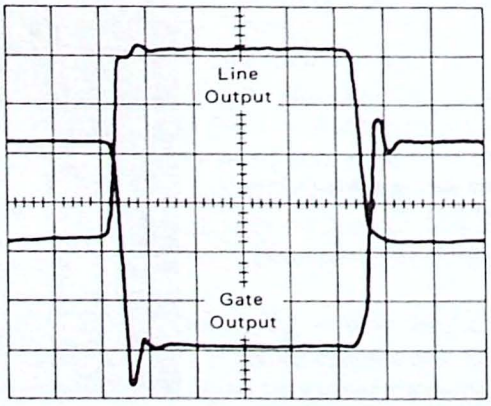
where ΔV_{INT} is the voltage drop in millivolts across the pulldown resistor when high, and n is the number of parallel series terminated lines.

When the waveform reaches the end of the line, the voltage will double to -260 millivolts and a reflection of -130 millivolts will be sent back toward the driving gate. Since the driving gate output is turned off, the reflection coefficient at the source is approximately 0.8. Therefore, after a time of twice the line delay, an additional -200 millivolts is received at the load. These reflections continue until the voltage at the end of the line reaches the logic Ø state.

These steps in voltage can be seen in the falling edge of the line output waveform (Figure 3-20), in close agreement with the calculations. The fall time increases by approximately six times the line propagation delay, or 7.2 ns. If the transmission line had been longer, the voltage step duration would have increased correspondingly. Note that the gate output at the end of the line also has an increased rise time and propagation delay.

Figure 3-21 shows the waveforms from the test setup shown in Figure 3-18, when only one line is driven (n = 1) and with R_E = 600 ohms. Using the equation

3-21: Waveforms from Test Set-Up of Figure 3-18 with Only One Line Driven (R_E = 600 ohm, n = 1)



Vertical Scale = 0.2 V/cm
Horizontal Scale = 10 ns/cm

for $R_{E(max)}$ gives a value of 680 ohms. Note that the rise and fall times are approximately equal (2 ns) meaning that the proper pulldown resistor was chosen. The rise and fall times at the line output are much faster in Figure 3-21 than in Figure 3-19, due to the lighter load at the gate output and reduced nodal capacitance at point A.

Analysis of series damping is very similar to that for a series terminated line. Differences are the line length and the value of the series damping resistor, R_S. For series damping this resistor value is normally smaller than the characteristic impedance of the line. Accordingly line lengths are permitted which are longer than the worst-case open line lengths ($R_S = 0$), as defined in Figures 3-13, 3-14, and 3-15. The same equations for voltage at point B and maximum R_E apply, as did for series terminated lines. In fact, series damping can be used to extend lines to any length, while limiting overshoot and undershoot to a predetermined amount. Figures 3-22 and 3-23 give minimum values of R_S for various line impedances for MECL 10,000 and MECL III. For these figures, overshoot was limited to 35% of signal swing and undershoot to 12%. The technique for calculating these R_S values is given in Chapter 7.

Here is an example of how Figure 3-22 and 3-23 can be used. Assume that a MECL III gate must drive a fanout of 2 (6.6 pF) at the end of 1 foot of line in the backplane. The characteristic impedance in the backplane is between 100 and 180

3-22: Minimum Values of R_S for Any Length of Line with Specified Limits of Overshoot and Undershoot, Using MECL 10,000

Z_o (OHMS)	MIN R_S (OHMS) FOR R_o = 15	UNDERSHOOT %	OVERSHOOT %
50	9	12	34.6
68	18	12	34.6
75	21	12	34.6
82	25	12	34.6
90	29	12	34.6
100	34	12	34.6
120	43	12	34.6
140	53	12	34.6
160	63	12	34.6
180	72	12	34.6

3-23: Minimum Values of R_S for Any Length of Line with Specified Limits of Overshoot and Undershoot, Using MECL III

Z_o (OHMS)	MIN R_S (OHMS) FOR R_o = 6	UNDERSHOOT %	OVERSHOOT %
50	18	12	34.6
68	27	12	34.6
75	30	12	34.6
82	34	12	34.6
90	38	12	34.6
100	43	12	34.6
120	52	12	34.6
140	62	12	34.6
160	72	12	34.6
180	81	12	34.6

ohms. An open line should not be used because it exceeds the length given in Figure 3-15: 0.6 in. Another method therefore must be used – coax, twisted pair, or series damped line.

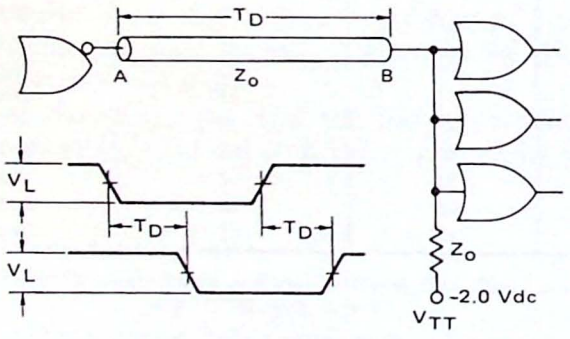
If series damping is used, then from Figure 3-23, a series damping resistor of 81 ohms or larger should be placed in the line at the driving end. The maximum value of the series damping resistor that should be used is 130 ohms for a fanout of 2, since there will be a dc level shift of 90 mV (maximum) caused by the series resistance in the line when the driving gate is in the high state. The 90 mV figure is based on the maximum input current, I_{inH}, of the MECL III (high Z) gate being 350 μA. (V = I·R, where R = 130Ω, and I = 2 x 350 μA).

Both the maximum overshoot and undershoot that can occur are given in the tables. If the proper value of R_S (series damping resistor) is used, as given in the tables, there is no restriction on line length or capacitance at the end of the line for the specified undershoot and overshoot. Of course, ohmic line losses and line propagation delay effects must be considered in the design.

Parallel Terminated Lines

Parallel terminated lines (Figure 3-24) are used for fastest circuit performance and for driving distributed loads. MECL 10,000 and MECL III are specified to drive "50 ohm lines." This refers to a line, terminated at the receiving end through a resistor of the characteristic line impedance to -2 volts from the V_{CC} supply. With parallel terminated lines, the line termination supplies the output pulldown. Consequently no other pulldown resistor is required at the output of the driving gate.

3-24: Driving a Parallel Terminated Line



The operation of the parallel terminated line is comparatively simple. The signal swing at point A is:

$$\Delta V_A = \Delta V_{INT} \left(\frac{Z_o}{R_o + Z_o} \right) .$$

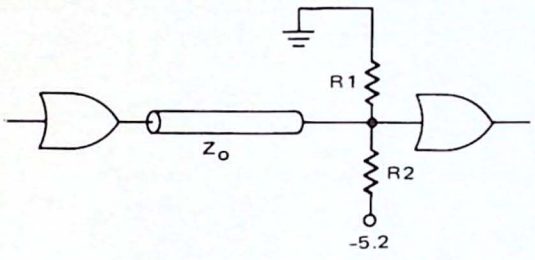
Since ΔV_{INT} is approximately 0.9 volts and the output impedance is low ($R_o \ll Z_o$), the signal swing at point B is typically greater than 800 millivolts. This signal propagates down the line, undistorted, in time T_D. Since the terminating resistor equals Z_o, there is no reflection and the sequence is ended.

An important feature of parallel termination is the undistorted waveform along the full length of the line. It should be noted that parallel termination can also be used with wire-wrap and backplane wiring where the characteristic impedance is not exactly defined. By approximating the characteristic impedance, the reflection coefficient ρ_L will be reasonably small, so overshoot and ringing will be held to within safe limits.

For large systems where total power is a consideration, the lines are normally terminated to a -2 Vdc supply. For power conservation, this is the most efficient manner of terminating MECL circuits. The drawback, of course, is the requirement of an additional supply voltage.

An alternate approach is to use two resistors in the way depicted in Figure 3-25. The Thevenin equivalent of these two resistors is one resistor equal to the

3-25: Parallel Termination with a Single Power Supply



THEVENIN EQUIVALENT RESISTORS FOR TERMINATION

Z_o (OHMS)	R1 (OHMS)	R2 (OHMS)
50	81	130
70	113	182
75	121	195
80	130	208
90	146	234
100	162	260
120	194	312
150	243	390

characteristic impedance of the line and terminated to -2 Vdc. R1 and R2 may be obtained as:

$$R_2 = 2.6\, Z_o$$

$$R_1 = \frac{R_2}{1.6}$$

Transmission Line Comparison

Since there are advantages to both series and parallel lines, the decision to use one or both methods in a system depends on the preference of the designer and on his system requirements. Figure 3-26 lists typical cases where terminations may be necessary, along with techniques which may be used.

Parallel terminated lines have the advantage when speed is the main factor. Loading a long line will not affect the propagation delay of the driving gate nor its edge speed, but loading does increase the propagation time of the signal down the line. It will be shown in Chapter 7 that the increase in delay time with loading is about twice as great for series damped lines as for parallel terminated lines. For short lines the capacitive load increases the propagation delay of the gate by slowing down the edges.

As mentioned previously, a big advantage of parallel termination is that the signal is undistorted along the full length of the line. When driving a large fanout, the loads may be distributed along the line with short stubs, instead of being lumped at the end of the line as is done with series termination. On the other hand, series

3-26: Types of Lines Recommended

SITUATION	PARALLEL TERMINATED LINE	SERIES TERMINATED LINE	OPEN LINE
1. Line lengths are shorter than specified (Fig. 3-13,-14,-15).	Yes	Yes	Yes
2. Driving gate drives 1 line, of length greater than specified (Fig. 3-13,-14,-15).	Yes	Yes	No
3. Driving gate drives 3 or more lines of lengths greater than specified (Fig. 3-13,-14,-15).	No	Yes	No
4. Gate loads must be distributed along a long transmission line.	Yes	No	No
5. Many gates are lumped at the end of long transmission line.	Yes	Yes	No
6. Only one power supply is to be used and the LOWEST power consumption is desired.	No	Yes	Yes
7. Two power supplies are used and the lowest power consumption is desired.	Yes	Yes	Yes
8. Backplane wire lengths are shorter than specified (Fig. 3-13,-14,-15).	Yes	Yes	Yes
9. Backplane wire lengths are longer than specified (Fig. 3-13,-14,-15). and a ground screen is used in backplane.	Yes (150 ohms)	Yes (100 ohms)	No
10. Backplane wire lengths are longer than specified (Fig. 3-13,-14,-15). (no ground screen is used).	Use Twisted Pairs, or Coax	No	No
11. Large temperature differentials exist between card bays or racks.	Use Twisted Pairs	No	No
12. Driving gate drives 3 or more lines in backplane longer than specified (Fig. 3-13,-14,-15).	No	Yes (100 ohms)	No
13. Wires are bundled closely together near noisy portion of system.	Use Coax or Twisted Pairs	Coax	No

termination has the ability to drive several parallel lines, as long as the drive current is compensated by the value of the output pulldown resistor. The MECL 10,000 and MECL III outputs will drive only one 50-ohm parallel terminated, or two 100-ohm parallel terminated lines. Exceptions to this rule include the MC10110 and MC10111 which have multiple gate outputs for driving three parallel 50 ohm lines.

Termination power is lowest for a parallel terminated line terminated to −2 Vdc. However, similar power savings may be realized by connecting the pulldown resistor for open wire or series terminated lines to −2 Vdc. Using a single power supply, the series termination and pulldown resistor uses less power than the two-resistor parallel termination. Typical power in the terminating resistors for 50 ohm lines for signals with 50% duty cycle is tabulated in Figure 3-27.

Additional information for calculating system power is contained in Chapter 5, "Power Distribution."

Crosstalk on circuit boards is normally not a problem with MECL, because the relationship of the signal line to the ground plane minimizes the energy coupled to adjacent lines. Even so, series terminated lines have less crosstalk than parallel terminated lines. The reason is that only one-half the logic swing is sent down the series terminated line. As a result the switched current is only one-half that of the larger, parallel terminated signal. This smaller signal energy results in less crosstalk.

3-27: Power Consumption for Various 50-Ohm-Line Terminations

TERMINATION SCHEME	RESISTOR ARRANGEMENT	RESISTOR POWER CONSUMPTION
Parallel	50 ohm to −2 Vdc	13 mW
Series	510 ohm to V_{EE}	30 mW
Parallel Combination	82 ohm to V_{CC}, and 130 ohm to V_{EE}	144 mW

Wirewrapped Cards

Wirewrapped cards can be used with both MECL II and MECL 10,000. The fast edge speeds (1 ns) of MECL III exceed the capabilities of normal wirewrapped connections. Mismatch at the connections causes a reflection which distorts the fast signal, reducing noise immunity significantly or causing erroneous operation. The mismatch remains with MECL II and MECL 10,000 but the distance between the wirewrap connection and the end of the line is well within the allowable stub-length distance, so the reflections cause no problem.

For lines longer than maximum allowable open line length for MECL 10,000 or MECL II, either series or parallel termination may be used. The parallel resistors are relatively high (typically 100 to 150 ohms) and are normally used only with MECL 10,000 because it can supply the output current required by the pulldown resistors. These resistors may be used with MECL II, but there will be a loss of approximately 100 millivolts noise immunity in the logic 1 state. Of course series damping resistors may be used with wirewrapped lines for both MECL II and MECL 10,000. Twisted pair lines may be used for longer distances across large wirewrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single-ended, or differentially using a line receiver.

Twisted pair line driving is an important feature of MECL circuits and is discussed in more detail in the next chapter. The recommended wirewrapped circuit cards have a ground plane on one side and a voltage plane on the other, to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wirewrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize crosstalk between parallel paths in the signal lines. Point-to-point wire routing is recommended because crosstalk will be minimized and line lengths will be shortest.

Production area for MECL Integrated Circuits

CHAPTER 4 System Interconnections

Signal connections between logic cards, card panels, and cabinets are important for obtaining the maximum system performance possible with MECL circuits. To understand how ringing and crosstalk affect system operation, it is helpful to review guaranteed noise margins, discussed in Chapter 1.

Noise margin is defined as the difference between a worst case input logic level and the worst case threshold closest to that logic level. Guaranteed noise margin (N.M.) for MECL 10,000 is:

$$NM_{1 \text{ level}} = V_{OHA \text{ min}} - V_{IHA \text{ min}}$$

$$= -0.980 \text{ V} - (-1.105 \text{ V}) = 125 \text{ mV};$$

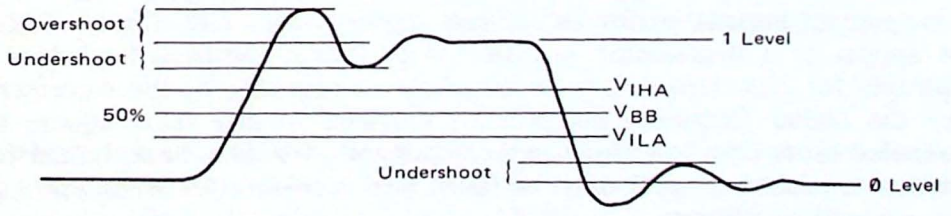
$$NM_{\emptyset \text{ level}} = V_{ILA \text{ max}} - V_{OLA \text{ max}}$$

$$= -1.475 \text{ V} - (-1.630 \text{ V}) = 155 \text{ mV}.$$

Thus, using the worst case design conditions, the circuits have 125 mV to guard against signal undershoot, and power or thermal disturbances. However, using *typical* logic levels of -0.900 volts and -1.700 volts, the circuit noise protection is typically greater than 200 mV for both the logic 1 and logic $\emptyset$ levels. Power and thermal design will be discussed in Chapters 5 and 6.

Good circuit interconnections should allow no more than 100 to 110 mV undershoot. The overshoot and undershoot waveform conventions are shown in Figure 4-1.

4-1: MECL Waveform Terminology



Both overshoot and undershoot are functions of many variables: line length, capacitive/inductive loading, rise time, and so on. Thus, in general, to maintain undershoot less than 110 mV requires one or more of the following:

- Reduction of system rise times;
- Reduction of interconnect line lengths;
- Use of matched, terminated transmission lines.

Reduction of rise time is easily accomplished by going to a slower MECL family, but this reduction in rise time may limit the use of the high bit rates and narrow pulse widths necessary for system performance goals. Interconnection line lengths are dictated by the system design and are routinely minimized as a matter of practice. Impedance matching of the interconnection lines remains then, the one variable which can be exploited for limiting the undershoot and ringing.

When using the faster varieties of MECL circuits, the type of card-to-card wiring in the system backplane area should be considered carefully. The initial decision is between two basic methods of board-to-board interconnect:

1. Controlled impedance, e.g., mother-daughter boards using microstrip lines, coax, ribbon flex, or twisted pair interconnects;
2. Uncontrolled impedance, e.g., open wire backplane wiring – with possible wide variations in characteristic impedance.

With MECL III, method 1 *must* be used. The entire system must be in a transmission line environment. While MECL 10,000 is designed to drive transmission lines, the slow edge speed allows it and MECL II to operate with the more economical wire over a ground plane layout. Wire over a ground plane or ground screen often has a characteristic impedance between 100 and 150 ohms, and can be series damped or parallel terminated for extended open wire lengths in the backplane area. Both wirewrapped and soldered wire connections are suitable for connecting wires to card connectors in MECL II or MECL 10,000 systems.

When designing system interconnections, four parameters must be taken into consideration:

- Propagation delay per unit length of line;
- Line attenuation;
- Crosstalk;
- Reflections due to mismatched impedance characteristics of the line, connectors, and line terminations.

Propagation delay of a line is important because unequal delays in parallel lines may cause timing errors. Also, for long lines the total delay time will often seriously affect system speed. Since the propagation delay of one foot of wire is approximately equal to the propagation delay of a MECL 10,000 gate, line length must be minimized when total propagation time is important.

Attenuation is also a parameter of a line. It varies with frequency and is seen as an increase in impedance for an increase in frequency. The effects of attenuation first appear as a degradation in edge speed. This is followed by a loss of signal amplitude for high frequencies on long lines. A rounding of the waveform occurs, since the higher frequency components required to give sharp square waves are attenuated more than low frequency components. Within a backplane attentuation is seldom a problem, but it must be taken into consideration when interconnecting among panels or cabinets.

Crosstalk is the undesired coupling of a signal on one wire to a nearby wire. Since a coupled pulse in the direction of undershoot results in a reduction of noise immunity, precautions should be taken to limit crosstalk. A good ground system and shielding are the best methods for limiting crosstalk. Differential twisted pair line interconnections can avoid problems caused by crosstalk by virtue of the common mode rejection of the receivers used with such an arrangement. Crosstalk is discussed in more detail under the heading "Parallel Wire Cables" later in this Chapter.

Reflections due to mismatched lines in system interconnections cause the same loss of noise immunity as discussed in Chapter 3 for printed circuit boards. The ability to terminate a line effectively is primarily a function of how constant the impedance is over the length of the line. Because it has high uniformity, coaxial cable is easier to terminate than open wire. Yet in many cases, twisted pair cable or ribbon cable may be purchased with specifications on the impedance of the line.

Connectors

There are very few high frequency edge connectors that do not cause waveshape distortion when rise times are under 1 ns. The few that don't are of the "matched impedance" type in which the on-board strip transmission line flows right into and out of the connector, without encountering a mismatch. Unfortunately, this form of connector is usually expensive and is often difficult to design with.

The only form of MECL logic that requires the use of matched edge connectors is the MECL III family. With rising edges slower than 2 ns, the MECL II and MECL 10,000 families may utilize conventional edge connectors. With them, very little mismatch occurs: typically < 20 mV.

Coaxial cable connectors that have near ideal characteristics over the bandwidths exhibited by MECL logic exist in a variety of types. The most popular are the BNC type and the subminiature SMA, SMB, or SMC types. The smaller miniature types offer direct microstrip to coaxial interconnects with low voltage standing wave ratio (VSWR), i.e. minimum reflection.

Coaxial Cable

Coaxial cable offers many advantages for distributing high frequency signals. The well defined and uniform characteristic impedance of the line permits easy matching. The ground shield on the cable minimizes crosstalk. Low attenuation at high frequencies makes good coaxial cable very desirable for handling the fast rise times associated with MECL signals.

The line bandwidths required for optimum MECL use are:

$$f = \frac{k}{t_r}, \qquad \text{where:} \quad k = 0.37^*, \quad t_r = \text{rise time;}$$

so: $$f = \frac{0.37}{1 \times 10^{-9}} = 370 \text{ MHz for MECL III with a 50 } \Omega \text{ load;}$$

and: $$f = \frac{0.37}{3.5 \times 10^{-9}} = 106 \text{ MHz for MECL 10,000 with a 50 } \Omega \text{ load.}$$

At MECL frequencies, skin effect is a primary cause of attenuation. Dielectric losses are insignificant below 1 GHz for the common dielectric materials – polyethylene or teflon. Attenuation due to skin effect is proportional to the square root of frequency and so may be plotted conveniently on log-log paper. Figure 4-2 contains data for three cable types tested. Maximum cable lengths recommended

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*O. Gene Gabbard, "High Speed Digital Logic for Satellite Communications." *Electro-Technology*, April 1969, p. 59.

with the various MECL logic families can be derived from these plots as the following example will show.

For maximum signal reductions of 100 mV in the 1 and Ø levels (i.e. a logic swing reduction from 800 mV p/p to 600 mV p/p) the permissible attenuation would be:

$$\text{Loss (dB)} = 20 \log\left(\frac{V_{in}}{V_o}\right) = 20 \log\left(\frac{0.8}{0.6}\right) = 2.5 \text{ dB}.$$

For MECL III with RG58/U the loss at 370 MHz is found to be 12 dB/100′ from Figure 4-2. Thus, with the 100 mV restriction:

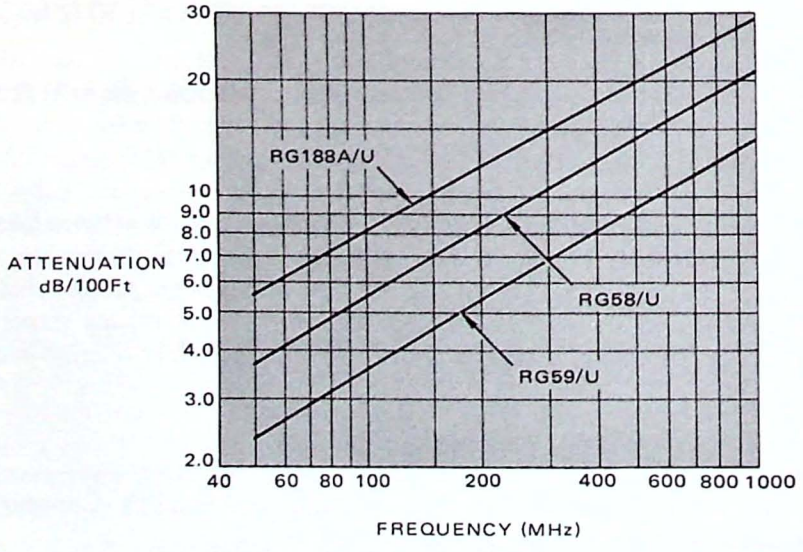
$$\text{Max Length} = 100 \text{ ft.} \cdot \left(\frac{2.5 \text{ dB}}{12 \text{ dB}}\right) = 20.8 \text{ ft.}$$

Figure 4-3 shows curves giving maximum line length as a function of operating frequency for the same three cable types used for Figure 4-2. Each curve assumes 2.5 dB permissible loss. It should be noted that a high bandwidth line is necessary to preserve fast signal edges, regardless of the bit rate of the system.

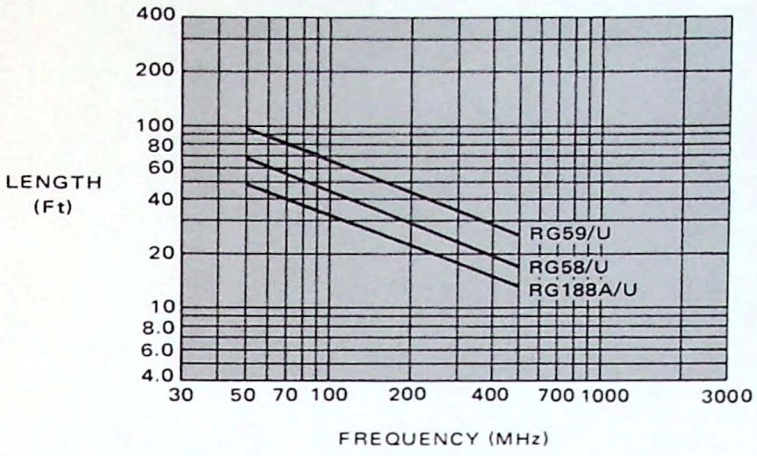
Figure 4-3 and the preceding calculations assume the coaxial line is properly terminated with a resistive load equal to the characteristic impedance of the line. The reactive component of the termination is of increasing importance at the high MECL III frequencies. At such frequencies, reactive elements can change the terminating impedance, thus causing reflections on the line. In addition, the effective inductance or capacitance would distort the output waveform, causing additional reflection down the line.

Standard carbon resistors were carefully measured at high frequencies to determine their reactive components. Results are listed in Figure 4-4. The effective circuit is a resistor with an inductor in series. Carbon resistors display more inductive

4-2: Coaxial Cable Attenuation versus Frequency



4-3: Coaxial Cable Length versus Operating Frequency: Constant 2.5 dB Loss Curves



TEST CONDITION	Z = R + jX
1/2 W, 51 ohms, 500 MHz	Z = 51.8 + j15.5
1/2 W, 51 ohms, 300 MHz	Z = 51.4 + j5.6
1/4 W, 51 ohms, 500 MHz	Z = 48.8 + j6.1
1/4 W, 51 ohms, 300 MHz	Z = 49.4 + j0.29
1/8 W, 51 ohms, 500 MHz	Z = 51.5 + j6.7
1/8 W, 51 ohms, 300 MHz	Z = 51.7 + j1.6

4-4: Impedance Characteristics of Carbon Resistors Measured on a GR Admittance Bridge

reactance as the resistor values become smaller, and display more capacitive reactance as the values get larger. However, 75 ohm resistors are normally close to being purely resistive.

The reflection at 300 MHz for a 50 ohm line using a 1/2-watt 51 ohm carbon resistor can be calculated:

$$\rho = \frac{Z_L - Z_o}{Z_L + Z_o},$$

where: Z_L = load impedance,

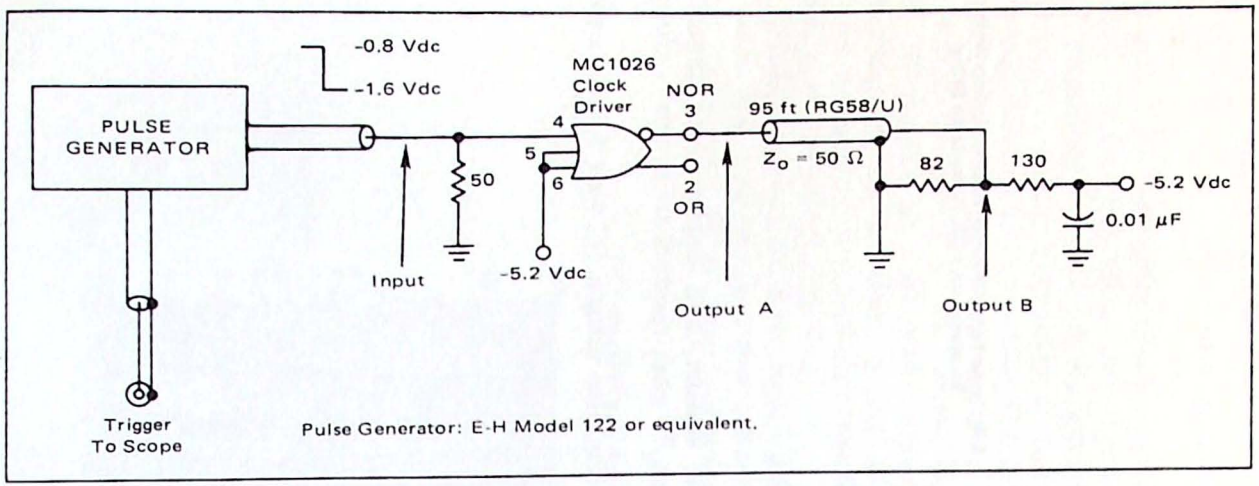
Z_o = line impedance;

so:
$$\rho = \frac{51.4 + j5.6 - 50}{51.4 + j5.6 + 50}.$$

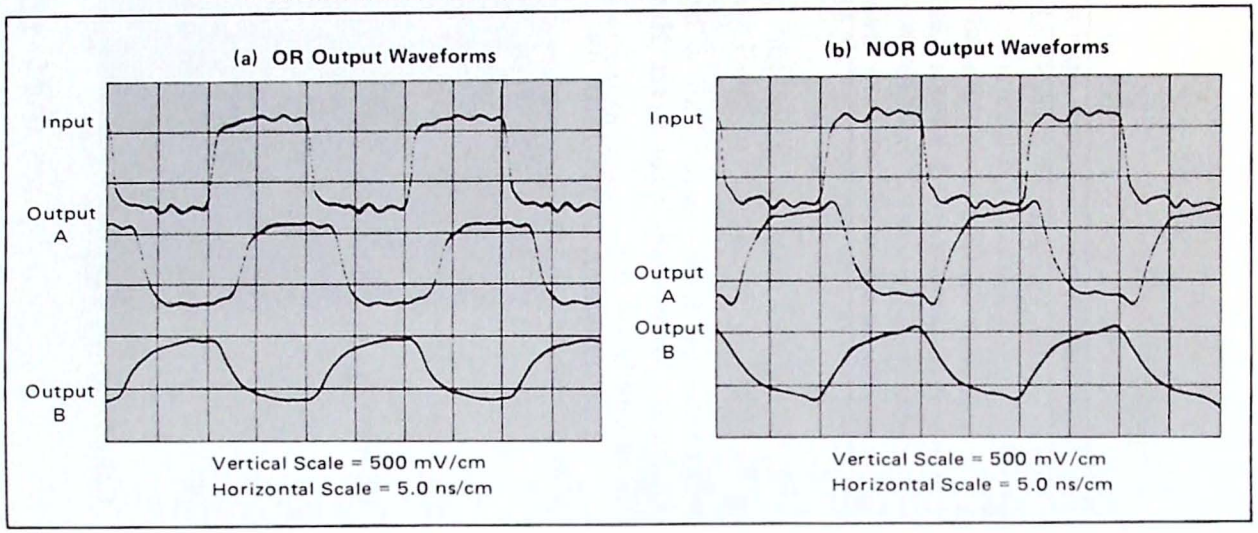
Calculations yield:

$$\rho = 0.055 \ \angle 72.8^\circ .$$

4-5: Line Driver Test Circuit



4-6: Line Driver Test Circuit Input and Outputs, Observed Via High Impedance 'Scope Probes.



4-7: Typical Switching Times

(Test Circuit Figure 3-5;
T_A = 25°C, f = 20 MHz)

Output A

TEST		TIME (ns)
OR		
t_{pd++}	(50% to 50%)	2.6
t_{pd--}	(50% to 50%)	2.7
t_r	(10% to 90%)	2.6
t_f	(90% to 10%)	2.0
NOR		
t_{pd+-}	(50% to 50%)	2.6
t_{pd-+}	(50% to 50%)	2.5
t_r	(10% to 90%)	2.4
t_f	(90% to 10%)	2.7

Output B

TEST		TIME (ns)
OR		
t_r	(10% to 80%)	3.8
	(10% to 90%)	5.4
t_f	(80% to 10%)	3.4
	(90% to 10%)	5.4
NOR		
t_r	(10% to 80%)	3.8
	(10% to 90%)	5.4
t_f	(80% to 10%)	3.7
	(90% to 10%)	5.7

As a result, (0.055) • (800 mV logic swing) = 44 mV, is reflected back down the transmission line. Clearly, this is much less than the 300 mV maximum overshoot recommended for safe MECL usage. With a slow repetition rate in relation to the propagation delay of the line (time per pulse $>3T_D$) the reflection appears as a small overshoot at the receiving end of the line. In high frequency operation the reflection may subtract from the transmitted signal. The amount would depend on the exact length of the line and the propagation velocity of the line. Subtracting signals appear to reduce the signal on the line, as if either the signal were attenuated, or as if the driving gate were bandwidth limited.

Standard carbon 1/8 watt resistors have been found to have good high frequency characteristics when used with MECL III. Either 1/8 or 1/4 watt resistors work well with MECL 10,000. When using precision wire wound or film resistors, care should be taken to determine the high frequency properties of these devices. Most wire wound and some film resistors become very inductive at high frequencies.

The fanout at the end of a coaxial line should also be limited at high frequencies because of reactive loading. At 300 MHz the fanout should be limited to four. The terminating resistor leads and circuit leads should be kept short. In many cases it is desirable to restrict long interconnecting cables to a fanout of one to minimize reflections and therefore to maintain a high degree of noise immunity.

The propagation velocity is very high in coaxial cable. Computing the propagation delay as:

$$t_{pd} = 1.017 \sqrt{e_r} \ ,$$

the delay for solid teflon and polyethylene insulated cables is 1.54 ns per foot (dielectric constant, $e_r \approx 2.3$). This compares with 2.2 ns per foot for stripline as calculated in Chapter 3. For maximum propagation velocity, coaxial cables with styrofoam or polystyrene beads in air dielectric may be used. However, many of these cables have high characteristic impedances and are slowed by capacitive loading. Nonetheless, coaxial cable definitely should be used when sending high repetition rate MECL signals over long lengths.

Illustrated in Figure 4-5 is a circuit used to test the performance of coaxial cable driven by an MC1026 clock driver. Figures 4-6 (a) and (b) show the waveforms of the circuit with 95 feet of RG58/U connecting cable. Output B in each figure clearly shows the waveform for a skin-effect limited line. Skin effect causes the waveform to rise sharply for the first 50% of the swing, then taper off during the remaining portion of the edge. Calculations show that the 10 to 90% waveform rise time is 30 times greater than the 0 to 50% rise time when the cable is skin effect limited. The output amplitude of the cable is at least 200 mV p/p less than the input, as would be expected from Figure 4-3.

Figure 4-7 presents the test results for the circuit in Figure 4-5. Notice that the numerical data show that at the output of the line, the time from 10 to 80% is much less than 10 to 90% – because of the coaxial skin effect. When operating within the limits discussed previously in this chapter, MECL signals are transmitted over coaxial lines with minimum distortion.

Differential Twisted Pair Lines and Receivers

Twisted pair line, differentially driven into an MECL line receiver (Figure 4-8), provides maximum noise immunity. This is because any noise coupled into a twisted pair line generally appears equally on both wires (common mode). Because the receiver responds only to the differences in voltage between the lines, crosstalk noise is ignored, since it is picked up equally by each of the two lines of the pair. This holds true up to the common mode noise rejection limit of the receiver. Quad line receivers, such as the MC1020 and MC1692, have +1 and -1.8 volt common mode rejection limits before the receiver's output approaches MECL input threshold levels. Common mode rejection can be improved to a -2.5 volt limit either by using a Schmitt trigger circuit (e.g. MC1035 or MC1065), or by using MECL 10,000 line receivers (e.g. MC10115 or MC10116).

With devices such as these four, the constant current source employed in the emitter node of the differential pair allows the increase in common mode rejection. This improvement is useful when signals are sent from circuits other than MECL. The MC1650 A/D Comparator is also used as a special purpose line receiver and offers ±2.5 volts common mode rejection. However the standard line receivers have more than adequate common mode noise rejection to handle any crosstalk between MECL signal lines. If higher voltage signal lines are run in parallel with MECL lines, shielded twisted pair lines may be used to reduce crosstalk further.

For low frequency operation, line length is limited by the dc resistance of the wire used and the voltage gain of the MC1020 line receiver. In order to determine line length allowed it is first necessary to examine the required signal at the end of the line, and the amplification possible with the receiver. The typical differential voltage gain of the MC1020 circuit (Figure 4-9) may be calculated. . .

Assume Q_2 is on, Q_3 is off. Then:

$$\text{gain} = g_m R_C .$$

R_C is known, and:

$$g_m = \frac{q\alpha I_E}{4KT},$$

where: $$-I_E = \frac{-V_{EE} - (V_{BB} - \text{base/emitter drop } Q_2)}{R_E}$$

$$I_E = \frac{-5.2 + 1.175 + 0.7}{1.18 \times 10^3} = 2.77 \text{ ma}$$

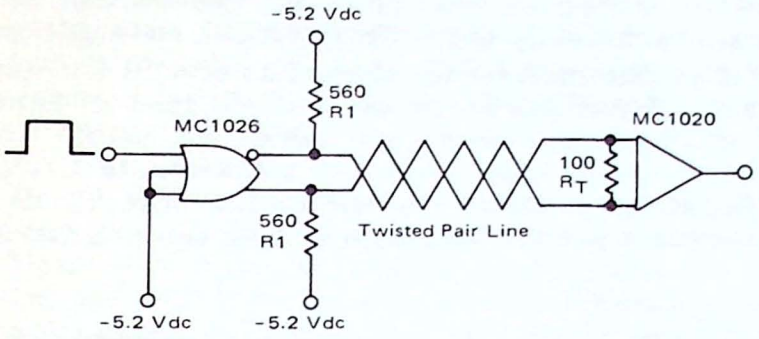
$$\alpha = \frac{\beta}{\beta + 1} \approx 1 \quad (\beta >> 1 \text{ for } Q_2),$$

K = Boltzmann constant = 1.38×10^{-23},

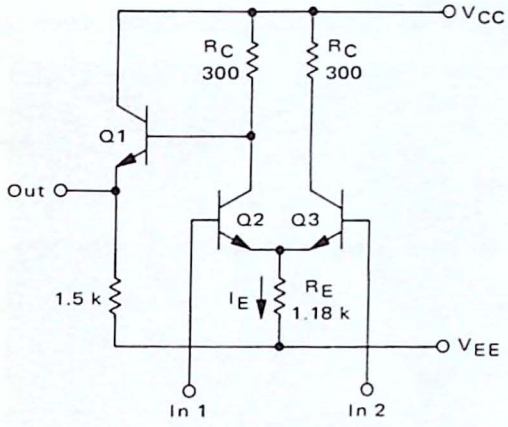
T = temperature degrees Kelvin $\approx$ 300,

and q = charge of electron = 1.602×10^{-19}.

4-8: Twisted-Pair Line Driver and Receiver



4-9: 1/4 MC1020 Schematic



Proceeding with the numerical calculations gives $g_m = 2.7 \cdot 10^{-2}$, and voltage gain = 8.3 V/V.

Allowing for 20% resistor tolerances, and temperature variations, the circuit gives a gain of at least 7 V/V. To obtain MECL level outputs, the minimum required input signal is 800 mV÷7 = 114mV (differential). Referring to Fig. 4-8, the voltage drop across the input terminating resistor, R_T is,

$$V_T = \overbrace{(V_{EE} - 1 \text{ logic level})}^{\text{net voltage}} \cdot \overbrace{\left(\frac{R_T}{R_1 + R_T + R_{Line}}\right)}^{\text{fraction across } R_T},$$

when resistor ratios determine the low level output.

For large R_T or R_{Line} values, the lower driver output limits at about 800 mV below the high output. For calculating maximum line resistance, use the relation:

$$V_T = |V_{OH} - V_{OL}| \cdot \frac{R_T}{R_T + R_{Line}}.$$

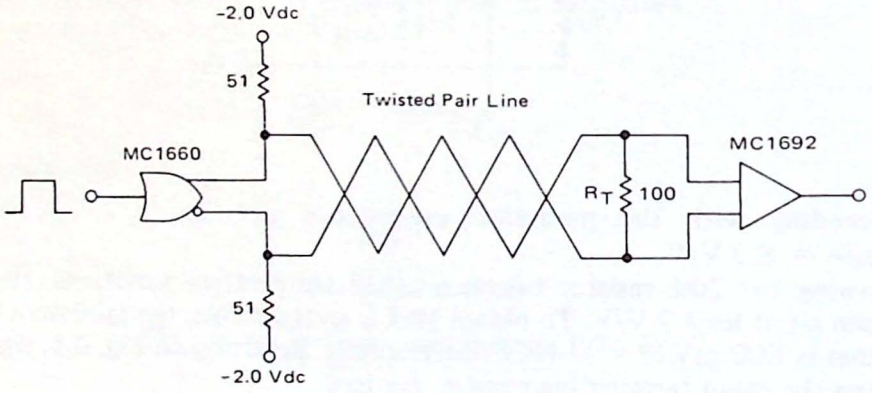
Setting V_T = 150 mV minimum for conservative operation, the maximum line resistance is found to be 433 ohms. The resistance of #24 AWG wire averages 26 ohms per 1000 feet, giving a theoretical permissible length of over 1.5 miles of wire. Clearly, the ac attenuation of the line will be the realistic limiting factor.

Figure 4-10 contains data for the attenuation of a 50 foot twisted pair line using the circuit of Figure 4-8. The voltage at R_T is the peak-to-peak voltage at either input. Although measurements were carried out to 200 MHz, use of the MC1020 is limited to around 70 MHz because of the bandwidth of its circuit. Driving and receiving the twisted pair line with the MECL III circuits as shown in Figure 4-11 yields the results in Figure 4-12. Comparison of the attenuation data in Figures 4-10

4-10: Attenuation of 50 Ft Twisted Pair Line with MC1026 Line Driver

FREQUENCY (MHz)	VOLTAGE AT R_T (mV)
50	320
75	320
100	280
125	240
150	210
175	160
200	140

4-11: MECL III Twisted Pair Line Driver and Receiver



4-12: Attenuation in a 50 Ft Twisted Pair Line with a MECL III Driver

FREQUENCY (MHz)	VOLTAGE AT R_T (mV)
50	380
75	340
100	320
125	280
150	250
175	180
200	160
225	150
250	140
275	120
300	100

4-13: Attenuation in a 10 Ft Twisted Pair Line with a MECL III Driver

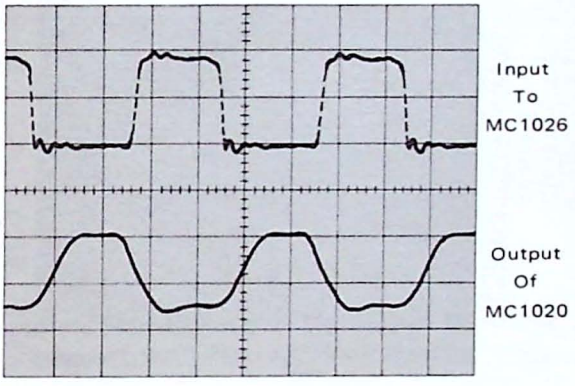
FREQUENCY (MHz)	VOLTAGE AT R_T (mV)
50	440
75	420
100	400
125	390
150	380
175	360
200	300
225	270
250	250
275	240
300	230

and 4-12 shows that the twisted pair line is bandwidth limited rather than limited by the MECL drivers. Reducing the line length to 10 feet of course results in less attenuation (cf Figure 4-13).

For very long lines the MECL II MC1020 line receiver will operate faster than the MECL III MC1692 receiver. The reason is that the voltage gain of the MC1020 is slightly higher than that of the MC1692. Driving a 1000 foot twisted pair line, the MC1020 would operate at 6.5 MHz with 600 mW output, while the MC1692 would be limited to 6.2 MHz for the same output.

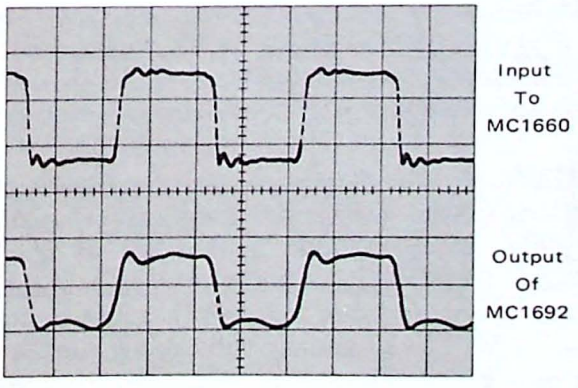
Despite the gain difference, as lines become shorter ($<<$ 1000 ft.), the MC1692 will switch faster, since the MC1020 displays *bandwidth* limitations when used on short lines. Figure 4-14 shows the behavior of the circuit of Figure 4-8 when driving a 50-foot line at 50 MHz. The 4 ns rise and fall times of the receiver can be seen at the output of the MC1020 receiver. The same line driven by the MECL III circuit of Figure 4-11 yields the waveforms of Figure 4-15. The faster switching

4-14: 50 Ft Twisted Pair Line at 50 MHz with MECL II



Horizontal Scale = 5.0 ns/cm (Both Traces)
Vertical Scale = 500 mV/cm (Both Traces)

4-15: 50 Ft Twisted Pair Line at 50 MHz with MECL III



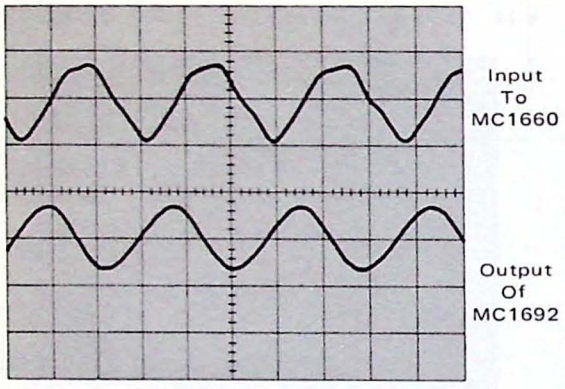
Horizontal Scale = 5.0 ns/cm (Both Traces)
Vertical Scale = 500 mV/cm (Both Traces)

times of MECL III are shown on the output of the MC1692. For both circuits, the propagation down the line is 70 ns for 50 feet of line. At best, overall circuit performance is improved only from 76 to 72 ns by using the faster MECL III.

However, the MECL III circuits do offer the big advantage of high rate capabilities on lines shorter than 10 feet. The result of driving twisted pair lines at high speed is shown by the waveforms in Figure 4-16. The traces were obtained for the circuit of Figure 4-11 driving a 10-foot line at 350 MHz. Both the attenuation of the line and the bandwidth of the MC1692 limit the output signal to about 650 mV, which is indeed still a useful MECL signal.

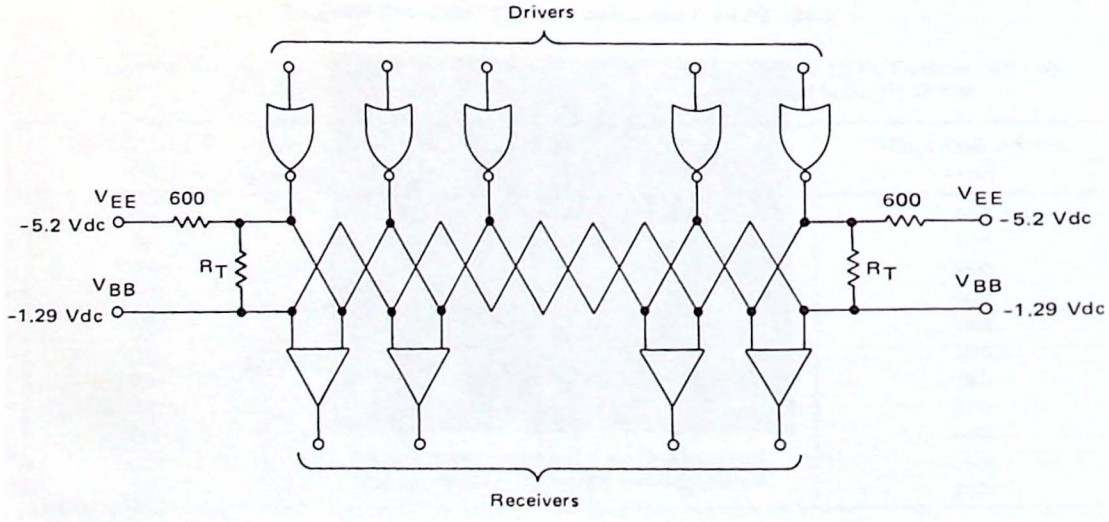
Party line operation over a single twisted pair line with MECL receivers may be used for saving space, for reducing connections and wiring, as well as to benefit from the party line two-way scheme. Figure 4-17 shows a method for using MECL in a data bus circuit. All driving gates are operating in a Wired-OR configuration

4-16: 10 Ft Twisted Pair Line Operated at 350 MHz with MECL III



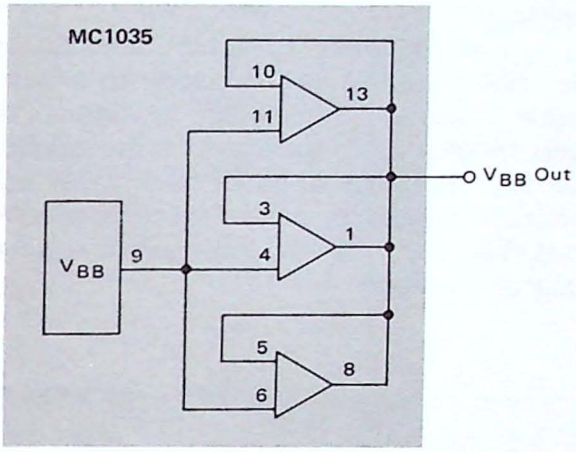
Horizontal Scale = 1.0 ns/cm (Both Traces)
Vertical Scale = 500 mV/cm (Both Traces)

4-17: Party Line Operation with MECL Line Drivers and Receivers



requiring that all drive gate outputs be held low when not sending data. (V_{BB} is available from the MC1035, MC10115, MC10116, and MC1692L and may be buffered as shown in Figure 4-18 to handle the necessary termination current).

All receivers operate in parallel. When driving long lines party-line style, it should be remembered that the receivers are operating single-ended. Consequently, the voltage gain is approximately one-half that for differential operation. Line attenuation must be computed accordingly. However, the advantages of crosstalk immunity deriving from common mode rejection of the differential line receiver remain. When stubbing off the data bus, the rules shown in Figures 3-13, 3-14, and 3-15 apply.



4-18: V_{BB} Generator

Twisted pair lines and line receivers offer several system advantages, when operating MECL circuits under adverse conditions. The following example is used to illustrate some of these advantages.

MECL II is specified to have a V_{OH} min of -0.850 volts and a V_{IH} min of -1.025 volts for a noise immunity of 175 mV, with both circuits at 25°C ambient temperature. However, if the driving gate is operating at 0°C, V_{OH} min is reduced to -0.895 volts; if the driven gate is operating at 75°C the V_{IH} min is increased to -0.950 volts; so the resultant noise immunity is reduced to 55 mV. To compound the worst case conditions, consider temperature and power supply changes also: if the driving gate is operated at a -5.46 volt supply (+5%) and 0°C temperature, the V_{OH} min is -0.891 volts. With the driven gate operating at a -4.94 volt supply voltage (-5%) and 75°C temperature, V_{IH} min is -0.920, giving a worst case noise immunity of 29 mV. Testing has shown that under these extreme conditions, worst case noise immunity in system usage is about 70 mV and circuits operating at typical levels have about 170 mV noise immunity.

However, this somewhat unrealistic example does illustrate the reduction in noise immunity under very adverse conditions. Any noise or voltage drop on the system ground would add to the loss of noise immunity. The example assumes MECL II signal levels, but similar conditions hold for MECL 10,000 and MECL III with the voltages changed to reflect the change in input voltage due to the bias point level, and the change in output voltage due to loading.

Line drivers operating differentially are not affected by the above conditions. The reduction of noise immunity to 29 mV (single-ended) is seen by a line driver

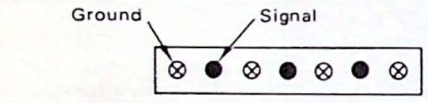
operated differentially, only as a small shift in the input levels – well within the acceptable limits of common mode operation. As a general rule, when operating MECL circuits at greatly differing temperatures or with differing supply voltage, or when the circuits are connected by a ground network with noise or voltage drop, the line driver should be used in the differential mode to retain maximum noise immunity.

Ribbon Cable

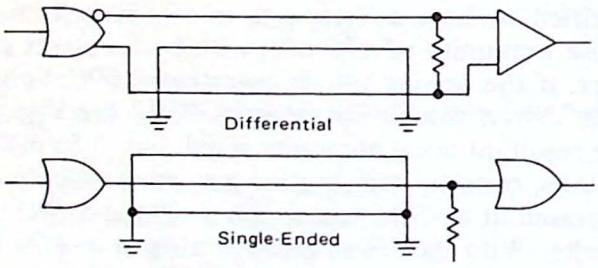
Ribbon cable is often used to interconnect MECL cards and panels. The advantages of ribbon cable include easy bonding to connectors because of the in-line arrangement of wires; and flexibility for use with hinged panels which swing open for servicing.

Two types of ribbon cable have been found to work well with the fast MECL circuits. One is the flat ribbon composed of several twisted pair lines. This twisted pair cable is operated differentially and should be received by one of the MECL line receivers. Single-ended operation is also possible by grounding one wire of the twisted pair. The conventional ribbon cable with side-by-side wires has a defined characteristic impedance only when every other wire is grounded as shown in Figure 4-19 (a). This cable may be driven either single-ended or differentially as shown in the examples in Figure 4-19 (b).

4-19: Ribbon Cable Interconnects



(a) Cross-Section



(b) Connections

Another type of multiconductor cable is called "triax." As its name suggests, this is a three-conductor cable with characteristics similar to coaxial cable. Triax has a flat cross section for flexibility, and may be used with all MECL families including MECL III. When using triax type cables, the manufacturer should be consulted for information about the impedance and attenuation characteristics of a specific cable type.

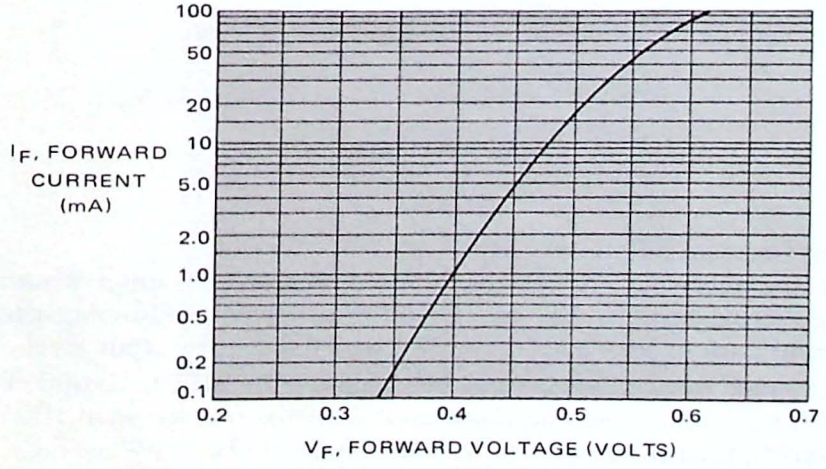
Schottky Diode Termination

Under certain board interface conditions, it may be advantageous to use a termination technique employing Schottky diodes. Several advantages are gained by the use of diode terminations:

- No matched impedance striplines are required;
- No line matching termination resistors are required;
- All signal overshoot is effectively clamped to the 1 or Ø logic level;
- All external noise in excess of 1 or Ø logic levels is clamped at the receiving gate or load;
- The total cost of layout, even though diodes are more expensive than resistors, may be less because no precise transmission line environment is necessary;
- If ringing is a problem on a drive line during system checkout, diode termination can be used to improve the waveform;
- Where line impedances are not well defined, as in breadboarding or prototype construction of systems using MECL, use of diode terminations is convenient and saves time.

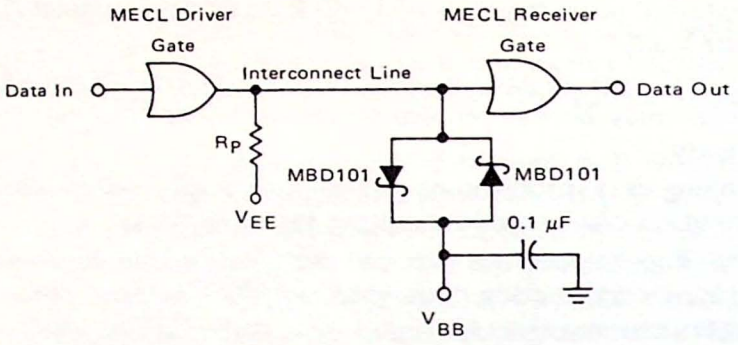
The forward conduction characteristic of the Schottky barrier diode is used to match the line impedance of the signal path. For instance, if a 90 ohm line is used, the diode impedance equals 90 ohms at a forward voltage of 0.45 volts ($\frac{0.45\ V}{5\ mA}$ from Figure 4-20). Therefore, the line would be terminated with only a small overshoot. The variable conduction curve of the diode permits terminating line impedances from 150 Ω to 50 Ω.

4-20: Schottky Diode MBD101 Forward Transfer Characteristic



In use (cf Figure 4-21), one side of the parallel diode network is biased at the MECL threshold V_{BB} (-1.29 volts for MECL 10,000 and MECL III). The V_{BB} source can be either a separate supply or a gate that supplies the required sink and source

4-21: Diode Termination



current (cf Figure 4-18). These current requirements can be determined from the graph in Figure 4-20 as follows:

$$V_{D1} \text{ (1 level diode drop)} = V_{BB} - \text{logic 1 level}$$

$$= -1.29 - (-0.90) = -0.39 \text{ V.}$$

From the graph in Figure 4-20, -0.39 V yields a diode current of approximately -1.0 mA (I_{BB1}), and:

$$V_{D\emptyset} \text{ (}\emptyset\text{ level diode drop)} = V_{BB} - \text{logic } \emptyset \text{ level}$$

$$= -1.29 - (1.70) = 0.41 \text{ V,}$$

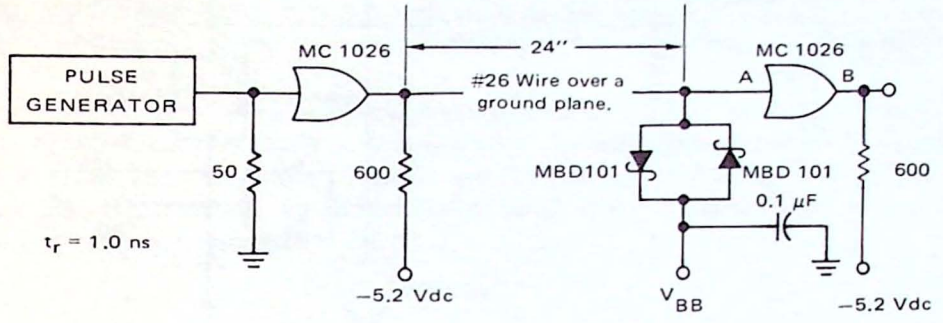
also indicating a current of 1.0 mA ($I_{BB\emptyset}$).

Thus at the receiving end of the line the power consumed would only be 0.4 mW. The driving device must have an emitter-follower pulldown resistor, Rp, to provide a current path to V_{EE} and to establish a well-defined output level.

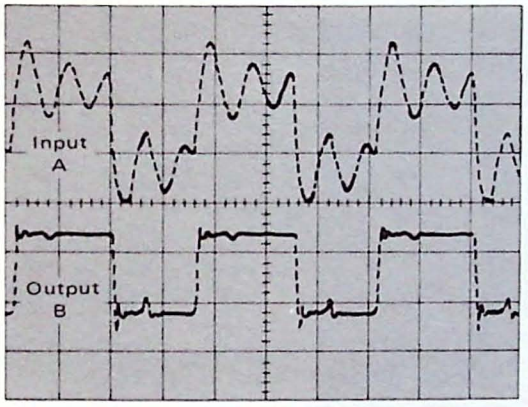
Consider a case when this resistor is 600 ohms, as for MECL 10,000. The power consumed in this resistor would be about 25 mW. If the resistor were 100 ohms to a V_{TT} of -2.0 volts, then the power consumed would only be 7 mW average.

A disadvantage of the diode termination scheme is that as many as three voltages might be required: V_{EE} (−5.2 V), V_{TT} (−2.0 V), and V_{BB} (−1.3 V).

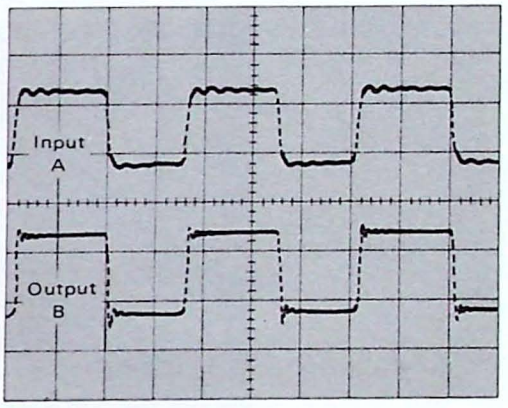
4-22: Circuit #1 – Reduction of Line Ringing by Use of Terminating Diodes



Without Diodes

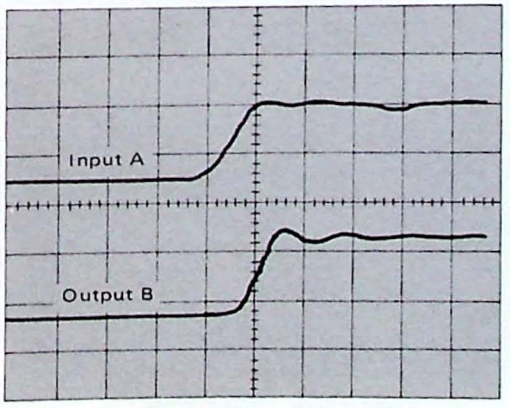


With Diodes



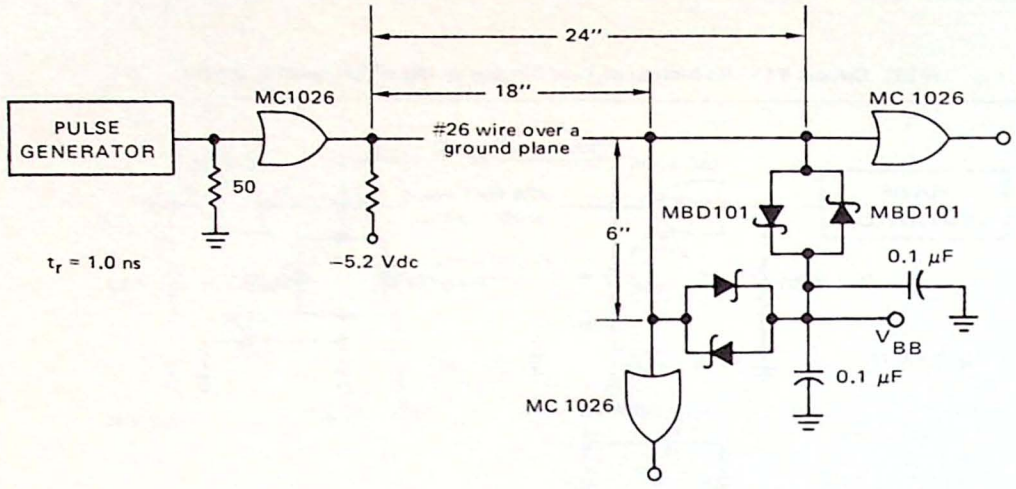
Vertical Scale = 500 mV/cm
Horizontal Scale = 20 ns/cm

Circuit Rise Time with Diodes

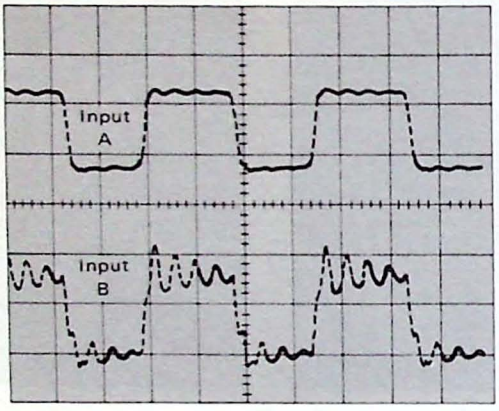


Vertical Scale = 500 mV/cm
Horizontal Scale = 2.0 ns/cm

4-23: Circuit #2 – Stub, off Diode Terminated Line

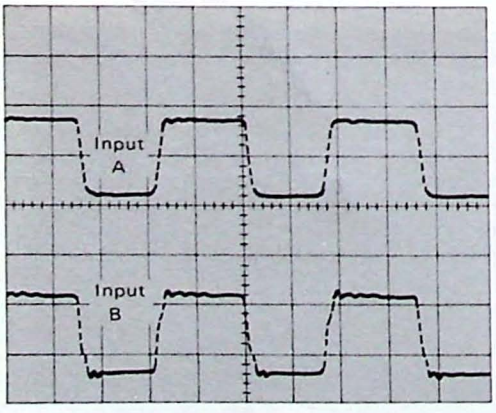


Without Diodes on Stub



Vertical Scale = 500 mV/cm
Horizontal Scale = 20 ns/cm

With Diodes on Stub



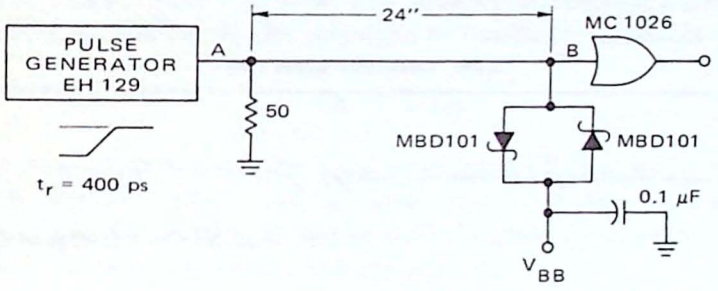
Vertical Scale = 500 mV/cm
Horizontal Scale = 20 ns/cm

Offsetting this are the elimination of the transmission line requirement, and the economical average termination power: (0.4 + 7.0) = 7.4 mW.

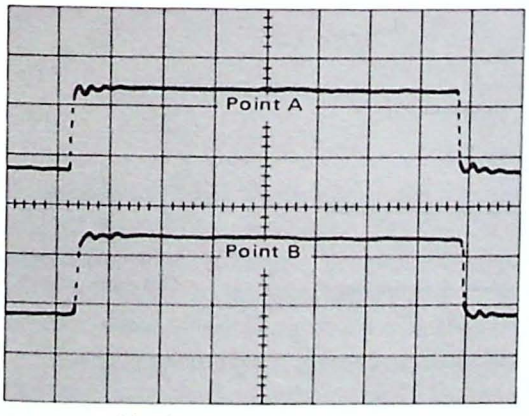
Figures 4-22 through 4-24 illustrate the performance of the Schottky diodes (MBD101) and show their unique ability to suppress severe ringing. Both circuit #1 (Figure 4-22) and circuit #2 (Figure 4-23) were evaluated with and without diode terminations. The 'scope traces show that ringing is reduced to less than 100 mV, while system rise time remains under 2.0 ns. Circuit #2 is a typical example of loads being stubbed off along a clock distribution line to provide clocking information to other parts of a system.

Even when dealing with subnanosecond risetimes (≈400 ps), Schottky diodes perform most satisfactorily – as shown by the waveforms derived from circuit #3 in Figure 4-24. The conclusion is that even for card-to-card or backplane interconnects, MECL III logic could be distributed with only a small amount of waveform degradation when diodes are used.

4-24: Circuit # 3 — Subnanosecond Performance of Diode Terminated Line

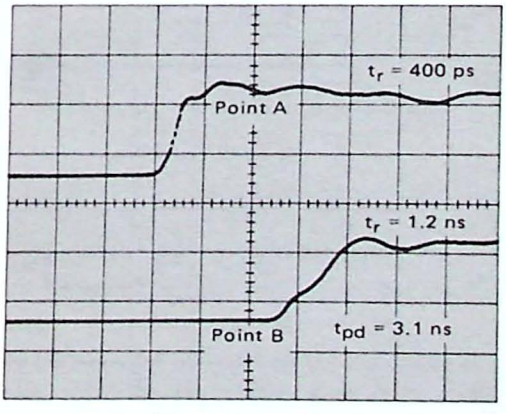


Line Input/Output Waveforms



Vertical Scale = 500 mV/cm
Horizontal Scale = 20 ns/cm

Waveform Rise Times

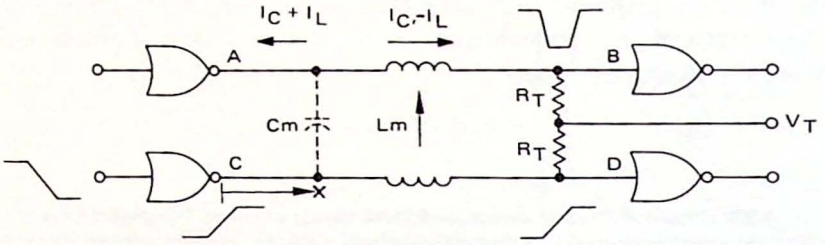


Vertical Scale = 500 mV/cm
Horizontal Scale = 1.0 ns/cm

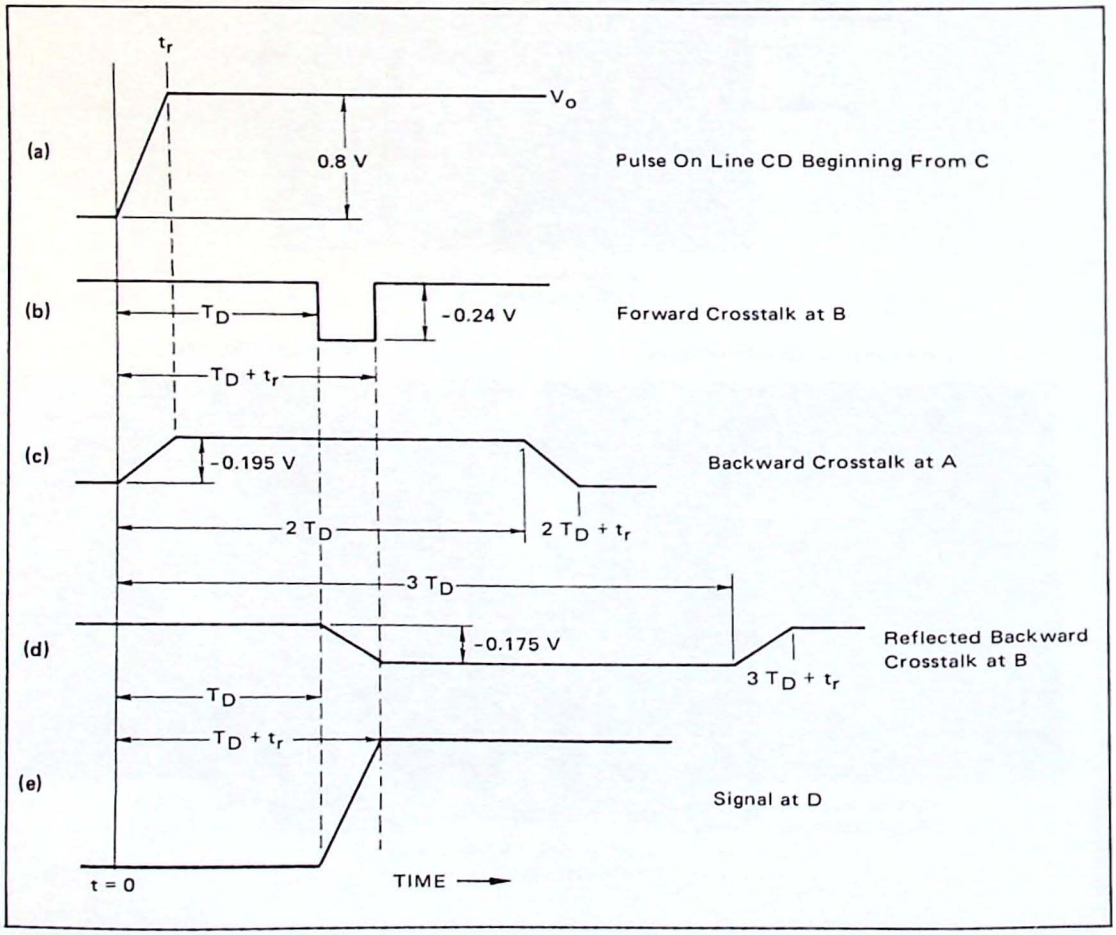
Parallel Wire Cables

Multiple conductor cables as purchased, or as constructed by lacing interconnection wires together, are not normally used with MECL because of crosstalk. Such crosstalk is due to capacitive and inductive coupling of signals among parallel lines as symbolized in Figure 4-25.

4-25: Crosstalk Coupling in Parallel Lines



4-26: Calculated Cross Talk



When a pulse propagating down line CD reaches any arbitrary point X, the signal is capacitively coupled into line AB. The coupled voltage on AB causes current (I_C) to flow from the point of coupling to both ends of the line.

Current in the direction of A is called "backward crosstalk" and that toward B is called "forward crosstalk." Coincident with capacitive coupling, the mutual inductance of the parallel lines also couples current (I_L) into line AB in the direction of backward crosstalk.

The total forward crosstalk is $I_C - I_L$ at point B. Since the parallel line coupling is primarily inductive, current flows from point B causing a negative pulse at that point (cf Figure 4-26). I_C and I_L are proportional in magnitude to the rate of change of the signal propagating from C (driving function). Coupling occurs only during the rise and fall times of the pulse as it propagates along CD.

Since the forward crosstalk propagates along AB at the same rate as the signal on CD, the result is a pulse at point B lasting for the duration of the rise time of the driving function. The amplitude of the resulting pulse is a function of the difference between inductive and capacitive coupling. Normally, the reflection of the backward crosstalk hides the small pulse at B.

Backward crosstalk current is $I_C + I_L$ and is a function of line length and velocity of propagation of the line. Backward crosstalk current starts at point A simultaneously with the signal at C. The coupling continues for the duration of the signal (T_D) on line CD; at time T_D the driving function is at point D, and also appears coupled to the other line at B. The backward crosstalk then requires another T_D to reach point A. Therefore the duration of backward crosstalk is:

$$T_B = 2\,T_D$$

The output impedance of the gate at point A (R_S) is low– typically 5 ohms compared with the line (Z_o = 75 to 150 ohms), so the backward crosstalk is reflected toward point B in proportion to the reflection coefficient.

Since the reflection coefficient for current, ρ_I, is:

$$\rho_I = \frac{Z_o - R_S}{Z_o + R_S},$$

if Z_0 = 100 ohms and R_S = 5 ohms, then:

$$\rho_I = +0.905\,.$$

The reflected backward crosstalk reaches point B at the same time the driven signal reaches point D, and is $2\,T_D$ in duration and about $0.9\,(I_C + I_L)$ in current amplitude. The positive reflection coefficient shows that the reflected current has the same polarity as the backward crosstalk. This reflection results in the pulse at point B (Figure 4-25) as shown in Figure 4-26d.

A similar analysis shows that if the gates at A and B were reversed so that the receiving gate and terminating resistor were at point A, the results would be similar. A positive crosstalk pulse would begin simultaneously with the driven signal at point C and have a duration of $2\,T_D$. The forward crosstalk would be reflected from the gate at point B and would not appear at point A until $2\,T_D$. This reflected signal is normally not seen as it occurs at the trailing edge of the backward crosstalk.

Crosstalk amplitude V (X,t) may be calculated with the following equation (cf reference 11, Chapter 7):

$$V(X,t) = K_f X \frac{d}{dt}\left[V_{in}(t - T_D\frac{X}{\ell})\right] + K_b\left[V_{in}(t - T_D\frac{X}{\ell}) - V_{in}(t - 2T_D + T_D\frac{X}{\ell})\right],$$

where:

K_f (forward crosstalk constant) $= -\frac{1}{2}\left(\frac{L_m}{Z_o} - C_m Z_o\right)$,

K_b (backward crosstalk constant) $= \frac{\ell}{4T_D}\left(\frac{L_m}{Z_o} + C_m Z_o\right)$,

L_m = mutual line inductance per unit length,
C_m = mutual line capacitance per unit length,
Z_o = characteristic line impedance,
ℓ = line length = 10 ft. for the following example,
X = arbitrary point along line,
t = arbitrary time,
T_D = total one-way line delay.

Also note that:

C_o = intrinsic line capacitance/unit length,
L_o = intrinsic line inductance/unit length.

Using the measured values $C_o \approx$ 1 pF/in, $L_o \approx$ 20 nH/in, $C_m \approx$ 0.446 pF/in, and $L_m \approx$ 10.3 nH/in for the cable under test, crosstalk can be calculated. The calculations can then be compared with test data on the cable.

First: $Z_o = \sqrt{\frac{L_o}{C_o}} = 141$ ohms,

and $t_{pd} = \sqrt{L_o C_o} = 0.14$ ns/in;

so: $T_D = 16.8$ ns.

Substituting values into the appropriate equations above gives:

$$K_f = -0.06 \text{ ns/ft},$$

and:

$$K_b = 0.244.$$

Proceeding now with the calculation of the forward crosstalk, V_f, in the line:

$$V_f(X,t) = K_f X \frac{d}{dt}\left[V_{in}\left(t - T_D\frac{X}{\ell}\right)\right],$$

where $V_{in}(t)$ may be represented by:

$$V_{in}(t) = \left(f_o(t) \cdot U(t)\right) - \left(f_o(t - t_r) \cdot U(t - t_r)\right).$$

Here U (t), the step function, has the values:

$$U(t) = 0, \text{ for all } t < 0,$$
$$U(t) = 1, \text{ for all } t \geq 0.$$

In this equation $f_o(t)$ describes the rising portion of the input pulse (Figure 4-26(a)), and since the pulse rises with a slope:

$$m \approx \frac{V_o}{t_r},$$

then the first term, $$f_o(t) = \frac{V_o}{T_r} \cdot t, \text{ for } t \geq 0,$$
$$= 0, \qquad \text{for } t < 0.$$

The second term,

$$f_o(t - t_r) \cdot U(t - t_r) = \frac{V_o}{t_r}(t - t_r), \text{ for } t \geq t_r,$$

$$= 0, \text{ for } t < t_r.$$

Note that the second term of $V_{in}(t)$ is zero until $t = t_r$. The U function is being used to "turn on" the first term at $t = 0$, and bring in the second term only for $t \geq t_r$:

Note that after time t_r, the function $V_{in}(t)$ remains at a value V_o, for all values of t.

Substituting $V_{in}(t)$ into the equation for $V_f(X,t)$, substituting $\left(t - T_D\frac{X}{\ell}\right)$ for t in $V_{in}(t)$, and evaluating at the end of the line ($X = \ell$), gives:

$$V_f(\ell, t) = K_f \ell \left\{\frac{d}{dt}\left[f_o(t - T_D)\, U(t - T_D)\right] - \right.$$

$$\left. \frac{d}{dt}\left[f_o(t - T_D - t_r)\, U(t - T_D - t_r)\right]\right\}$$

$$= K_f \ell \left[\frac{V_o}{t_r}\right] \cdot \left[U(t - T_D) - U\left(t - (T_D + t_r)\right)\right].$$

This gives a pulse at point B equal in duration to the driven line rise time, t_r, and starting at time T_D as shown in Figure 4-26(b). The amplitude of this pulse is, for a rise time $t_r = 2$ ns, at point B ($t = T_D$):

$$V_f(B) = \frac{K_f \ell V_o}{t_r} = \frac{(-0.06)(10)(0.8)}{2} = -0.24 \text{ volt.}$$

The backward crosstalk is calculated as follows:

$$V_b(X,t) = K_b \left[V_{in}\left(t - \frac{T_D X}{\ell}\right) - V_{in}\left(t - 2T_D + \frac{T_D X}{\ell}\right) \right].$$

For the same ramp function, $f_o(t) = \frac{V_o}{T_r} \cdot t$, as used with the forward crosstalk.

Taking $X = 0$ for point A:

$$V_b(0,t) = K_b \left[V_{in}(t) - V_{in}(t - 2T_D) \right],$$

$$V_b(t) = K_b \left(\frac{V_o}{t_r}\right) \Big[tU(t) - (t - t_r)U(t - t_r) -$$

$$(t - 2T_D)U(t - 2T_D) + (t - t_r - 2T_D)$$

$$U(t - t_r - 2T_D) \Big].$$

This gives a pulse at point A starting simultaneously with the driving signal at point C. The leading edge of the backward crosstalk pulse (Figure 4-23(c)) is a ramp until time t_r. The pulse levels off until time $2T_D$ then slopes to the starting point at time $2T_D + t_r$. The amplitude of this pulse is:

$$V_b(A) = K_b V_o = 0.244(0.8) = 0.195 \text{ volt.}$$

These calculations assume the 10 foot line is terminated in its characteristic impedance at points D and B. However, since the gate output at point A of Figure 4-25 is a low impedance, only a small voltage pulse is seen at the MECL gate. As previously discussed, 90% of the backward crosstalk is reflected to point B. The amount of crosstalk at point B due to reflected backward crosstalk is calculated to be: $(-0.9)(0.195) = -0.175$ volts as shown in Figure 4-26(d).

Figure 4-27 lists measured crosstalk in a ten foot multiconductor cable for the test circuit of Figure 4-28. Using all wires in the cable for signal lines causes a prohibitive amount of crosstalk, as shown.

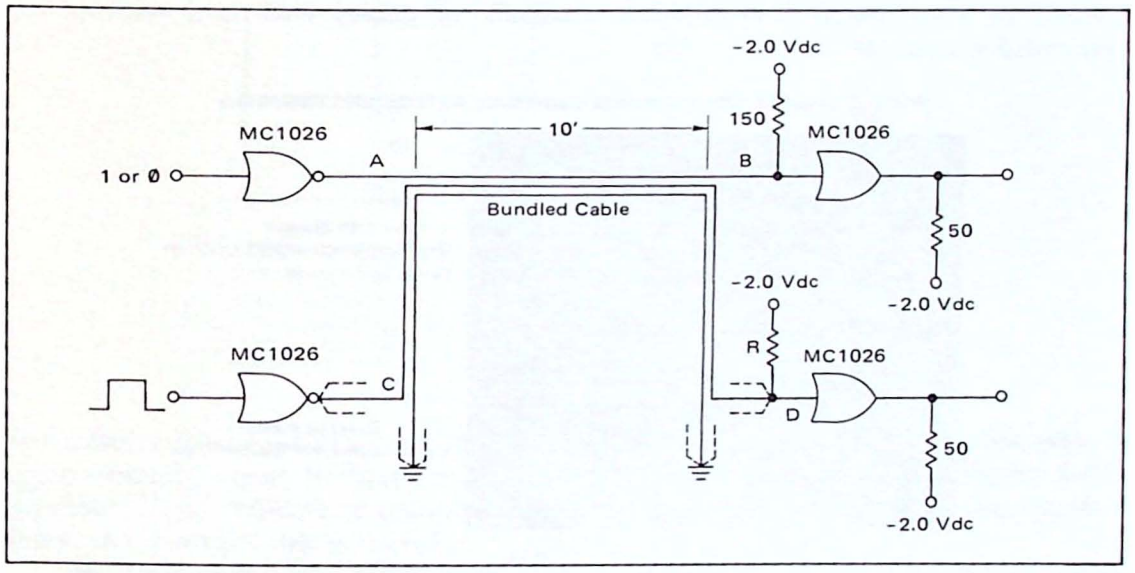
Several factors contribute to the discrepancy between calculated and measured crosstalk. The characteristic impedance of the line is comparatively undefined

4-27: 10 Ft. Multiple Conductor Cable Crosstalk

CONDUCTORS AT C	CROSSTALK AT B (mV)	R (OHMS)
① 1	240	150
2	360	75
3	420	50
1*	60	150
2**	80	75
3***	100	50

*With one wire in cable grounded at both ends
**With two wires in cable grounded at both ends
***With three wires in cable grounded at both ends
① Compare with theoretically calculated example.

4-28: Cross Talk Test Circuit



because there is not a solid ground reference for the cable. Thus, placement of the cable with respect to the system ground and other cables affects the characteristic impedance. In addition, capacitive and inductive coupling will vary along the cable due to the relative location of wires with respect to each other. The one other factor not allowed for in the calculations is attentuation in the line which damps out the higher frequency components of the signal, slowing the rise time of the signal as it propagates along the line.

The 150 ohm terminating resistor gives an approximate impedance match, to cut down overshoot and ringing. However, residual mismatch causes reflections to return along the line. Such reflections interfere with the signal by producing distortion at the receiving gate input, and so limiting high speed operation of the cable. Serious distortion occurs when the reflected signal coincides with a following signal, i.e. when the transmitted frequency equals:

$$\text{Frequency} = \frac{1}{2\,T_D}.$$

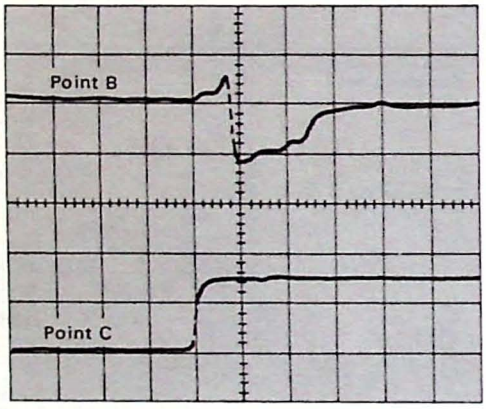
For the 10 foot line example just discussed:

$$f = \frac{1}{2\,(16.8)} = 29.8\ \text{MHz}.$$

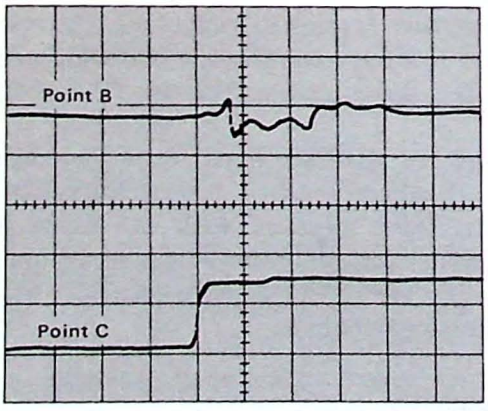
Test data coincides with the calculated performance to indicate that serious distortion occurs around 30 MHz in the 10 foot cable. The previously computed propagation speed of 1.68 ns/ft also closely agrees with the measured time of 1.65 ns/ft.

Crosstalk is reduced by supplying a ground reference in the cable. In a multiconductor cable this may be done by grounding approximately the same number of wires in the cable as there are signal lines. This measure reduces crosstalk by a factor of 4 (cf Figure 4-27). Figures 4-29 and 4-30 show the crosstalk in the circuit of Figure 4-28, and compare crosstalk of cables with and without one grounded wire in the cable.

4-29: Crosstalk in Multiconductor Cable with No Grounded Conductor



4-30: Crosstalk in Multiconductor Cable with One Grounded Conductor



The amplitude of crosstalk is independent of length for "long lines." Defining a long line as having a propagation delay greater than 1/2 the input rise time gives a "long line" length of 0.605 ft. for a 2 ns rise time waveshape:

$$\text{Long Line Length} \geq \frac{t_r}{2\,t_{pd}}$$

$$= \frac{2}{(1.65)\,(2)} = 0.605 \text{ ft. (for the cable just discussed).}$$

4-31: Test Results for an 18 Inch Multiple Conductor Cable: Crosstalk

CONDUCTORS AT C	CROSSTALK AT B (mV)	R (OHMS)
1	240	150
2	350	75
3	400	50
1*	70	150
2**	80	75
3***	100	50

*With one wire in the cable grounded at both ends.
**With two wires in the cable grounded at both ends.
***With three wires in the cable grounded at both ends.

Test results (Figure 4-31) show that crosstalk for an 18 inch multiconductor cable is approximately equal to that for the 10 foot bundled cable shown in Figure 4-27. However, since reflections damp-out much faster because of the lesser propagation delay, the shorter cable is useful to 100 MHz.

Multiple conductor cables of this type (bundled) may be used successfully with MECL II or MECL 10,000 if one-half the wires are grounded at both ends. However, the 100 mV of crosstalk present with the grounded lines significantly reduces noise immunity. The cable is also susceptible to external signals coupling to the entire cable. These cause additional noise on the line. Thus, this cable should be used only when cost or manufacturing techniques require it. Other cable types – coaxial, tri-axial, ribbon, or twisted pair – are recommended wherever possible.

Twisted Pair Cable, Driven Single-Ended

Cables formed of twisted pair lines have a more defined characteristic impedance than parallel wires. So, twisted pair can be terminated more accurately at the receiving end, reducing reflections. Further, the speed of operation of twisted pair is limited by attenuation rather than by any significant reflection interference. Test results show a 10 foot length of twisted pair cable may be used up to 70 MHz before attenuation reduces noise immunity by 100 mV. Propagation delay is the same as for parallel lines – 1.65 ns/ft.

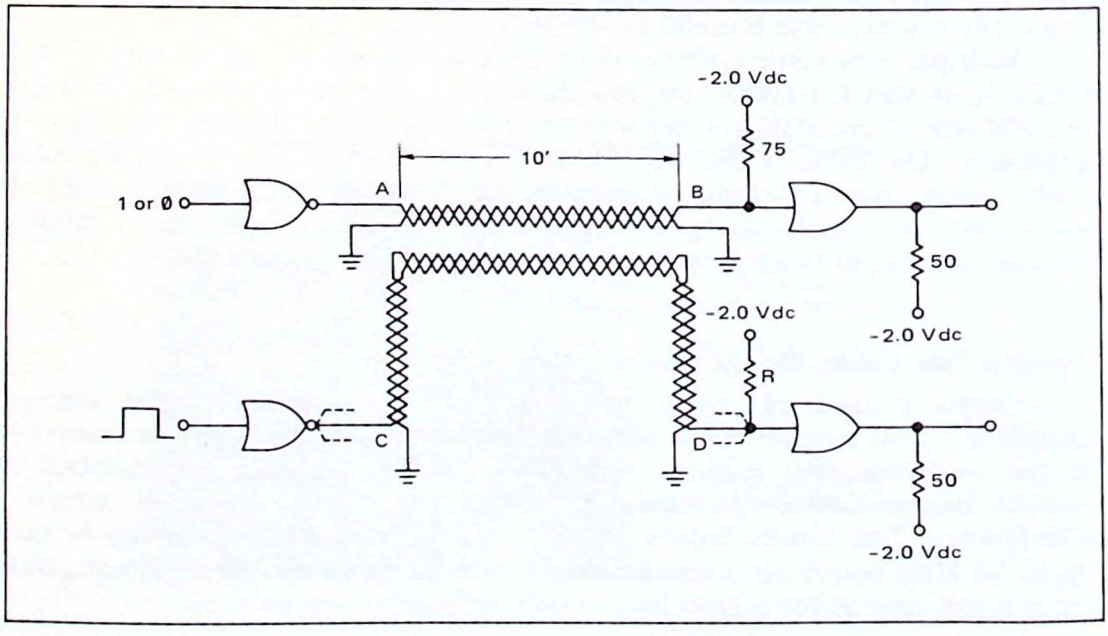
Crosstalk for the twisted pair cable is comparable to that for the parallel wire cable operated with half the leads grounded. This is because the higher switching current (due to lower Z_0 of twisted pair) offsets the better ground of the twisted pair. Crosstalk magnitude in a twisted pair cable is listed in Figure 4-32 for the test circuit of Figure 4-33. If shielded twisted pair cable is used, crosstalk is significantly reduced (compared to unshielded) as shown in Figure 4-34 and Figure 4-35. Both ends of the shield as well as the second wire of the pair were grounded in the test whose results are shown in Figure 4-34.

4-32: Crosstalk for 10 Ft Multiple Twisted Pair Cable

CONDUCTORS AT C	CROSSTALK AT B (mV)	R (OHMS)
1	60	75
2	80	39
3	90	27

Differential operation of twisted pair line offers advantages over the standard multiconductor cable when sending higher frequency signals. When operated single-ended (as shown in Figure 4-33), twisted pair is still susceptible to noise external to the cable. Any noise coupled into the entire cable causes a direct reduction of noise immunity.

4-33: Twisted Pair Crosstalk Test Circuit

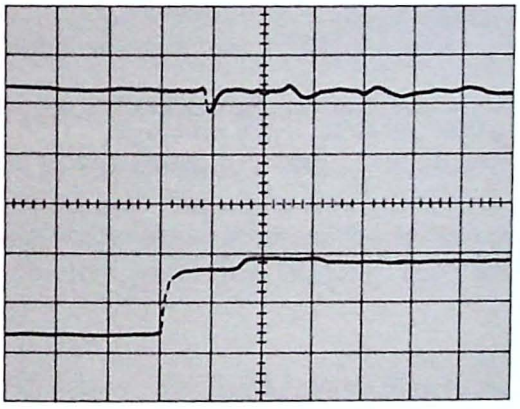


Since one-half the wires in a multiconductor cable should be grounded for low crosstalk (comparable to the twisted pair), cable density is the same for both – two wires per signal path. The use of shielded twisted pair significantly reduces crosstalk and should be used in applications where crosstalk could be a problem. Differential operation of twisted pair lines is *definitely preferred* over single-ended twisted pairs for sending MECL signals between sections of a system.

4-34: Crosstalk for 10 Ft Multiple Shielded Twisted Pair

CONDUCTORS AT C	CROSSTALK AT B (mV)	R (OHMS)
1	30	75
2	30	39
3	40	27

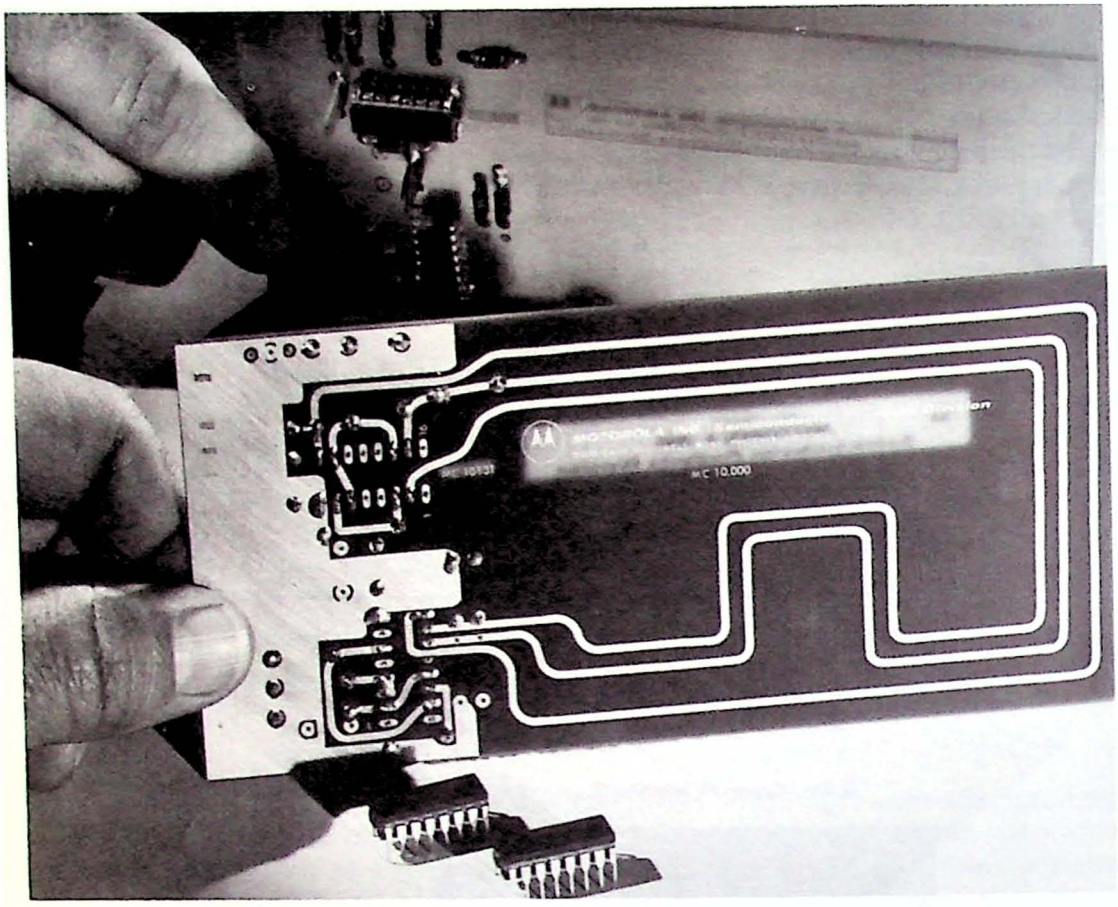
4-35: Crosstalk in a Multiconductor Shielded Twisted Pair Cable



Crosstalk
Vertical Scale = 100 mV/cm

Driving Signal
Vertical Scale = 500 mV/cm

Horizontal Scale = 20 ns/cm (Both Traces)



Conventional two-sided printed circuit board can be used when designing with MECL 10,000. Shown is a demonstration board which illustrates some of the capabilities of MECL 10,000 series parts.

The circuit consists of a ring oscillator and a divide by four counter, connected by a 12 inch microstrip line. Operating frequency is 83 MHz.

Together with an oscilloscope, the circuit illustrates propagation delay, edge speed, and synchronous flip-flop performance, as well as series, parallel and non-terminated line connections.

CHAPTER 5 Power Distribution

Power distribution is an important factor in system design. The loss of noise margin due to reduced power supply voltage or noise on the power supply lines means a reduction in the circuit tolerance to crosstalk and ringing as discussed in Chapters 3 and 4. Points to consider for overall system operation include total circuit and termination power, voltage drops on the power buses, and noise induced on the power distribution lines by the circuits and by external sources.

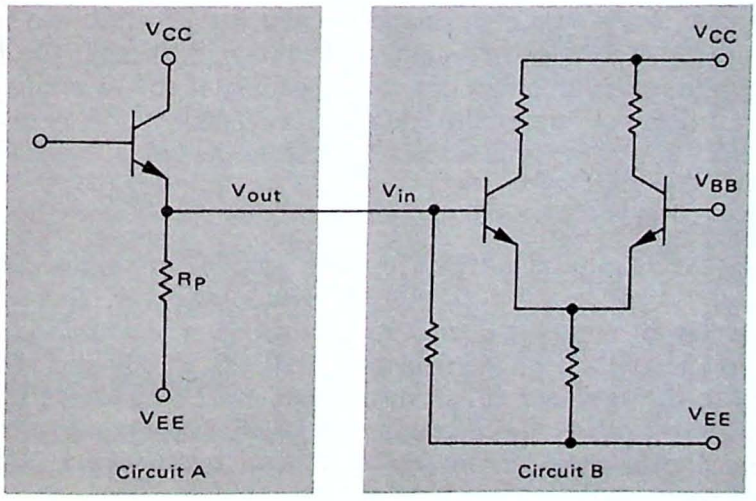
MECL circuits are designed to interface with each other over a wide power supply voltage range – at least ±10% from the nominal -5.2 volts, – without loss of noise margin (other than that due to reduced signal swing at low voltage). However, if two circuits are at different supply voltages or on the same power supply with a voltage offset between circuits, there will be a predictable loss of noise margin.

Figure 5-1 illustrates supply points for two MECL circuits (A and B). The MECL circuits are most sensitive to voltage differences between V_{CC}s for the two circuits. Any voltage drop on this power bus causes a direct loss of noise immunity and should be avoided. Similarly, any noise on the V_{CC} line not common to both circuits may subtract from noise immunity. For this reason, V_{CC} is normally made to be the system ground – usually the most stable reference level in the system.

The main causes of V_{CC} offsets between circuits are:

- inadequate power buses to handle the current;
- separate supplies with common negative terminals operating at slightly different voltages (not recommended for system design);
- separate positive grounded supplies with inadequate interconnecting ground bus bars.

5-1: MECL Power Points



5-2: Changes in Output Levels and V_{BB} with V_{EE}

VOLTAGE	MECL II	MECL 10,000	MECL III
$\Delta V_{OH}/\Delta V_{EE}$	0.015	0.016	0.033
$\Delta V_{OL}/\Delta V_{EE}$	0.230	0.25	0.27
$\Delta V_{BB}/\Delta V_{EE}$	0.115	0.148	0.14

A more common problem is with circuits which have a good ground, but which operate with different V_{EE} voltages. The loss of noise margin can be calculated from the changes in V_{OH}, V_{OL}, and V_{BB} as functions of supply voltage. Figure 5-2 shows the change in these levels as a function of V_{EE} for the MECL families. The change in the logic 1 output level is very small compared to the change in logic ∅ as a function of V_{EE}. V_{BB} is designed to change at one-half the logic ∅ rate, to stay at the center of the logic swing.

The following example illustrates the loss of noise margin due to circuits operating at largely differing voltages. Worst case MECL 10,000 Series logic levels are used in the example.

If the driving gate is at –5.46 volts (+5% of nominal), the output levels are:

$$V_{OHA\ min} = (-0.980) - (0.016)(5.2)(0.05) = -0.984 \text{ volts},$$

$$V_{OLA\ max} = (-1.630) - (0.25)(5.2)(0.05) = -1.695 \text{ volts}.$$

If the receiving gate is at –4.94 volts (–5% of nominal), the input levels are:

$$V_{IHA\ min} = -1.105 + (0.15)(5.2)(0.05) = -1.066 \text{ volts},$$

$$V_{ILA\ max} = -1.475 + (0.15)(5.2)(0.05) = -1.436 \text{ volts}.$$

Worst case noise margin is therefore:

Logic 1: 1.066 - 0.984 = 0.082 volts,

Logic ∅: 1.695 - 1.436 = 0.259 volts.

In this example, worst case noise margin in the logic 1 state was reduced from 125 mV to 82 mV by a 10% power supply difference. Although the logic ∅ noise margin here improved, it would in fact have been reduced if the receiving gate were at the +5% supply voltage. Since the example assumed worst case voltages, an additional 100 mV protection from noise could be expected in typical system use.

System Power Calculations

The total power required by MECL circuits consists of several parts: current switch, bias supply (V_{BB}), output emitter follower transistor, and terminating or pulldown resistor power. Since the output emitter follower power and resistor power are dependent on the method of termination for MECL 10,000 and MECL III, they are not included in the specified circuit power and must be added for total system power. The data sheet power specifications for MECL II parts *are* representative of system requirements, because the internal pulldown resistors are included in the determination of package power.

Gate power is calculated as the sum of the powers for each of the three sections illustrated for the basic MECL 10,000 gate (Figure 1-1). The bias driver, which furnishes -1.29 volts to the base of Q5, dissipates about 5 mW/gate, as may be seen from the following:

$$I_{BB} = \frac{V_{EE} - V_{BB} - \text{diode drop (0.79 V)}}{R_{BQ6}} = -0.625 \text{ mA}$$

so: $P_{BB1} = I_{BB} \cdot V_{EE} = 3.24$ mW (shared by 2 gates);

and: $$I_{Q6} = \frac{V_{EE} - V_{BB}}{R_{EQ6}} = -0.64 \text{ mA},$$

$$P_{BB2} = I_{Q6} \cdot V_{EE} = 3.32 \text{ mW};$$

$$P_{TOTAL\ BIAS} = \frac{P_{BB1}}{2} + P_{BB2} = 4.94 \text{ mW},$$

per gate in a gate pair. For a single gate, the bias power is not shared, so the total power for a single gate would be 6.56 mW.

Current switch power can be calculated in a similar fashion:

$$I_{EQ5} = \frac{V_{EE} - V_{BB} - \text{diode drop (0.79 V)}}{R_E} = -3.99 \text{ mA};$$

$$P_{Q5} = I_{EQ5} \cdot V_{EE} = 20.8 \text{ mW}.$$

For one gate, the combined power dissipation would be: 20.8 mW + 6.6 mW = 27.4 mW. However, the actual power dissipation is less than this on a package basis, because the gates share a common bias driver, which is coupled through emitter followers for isolation. A quad gate, for example, has a typical per gate dissipation of 25 mW. Note that this power is constant over the full speed range of operation. Transistor base currents were omitted from the above calculations as they are beta dependent and have little effect on package power.

Typical input power may be computed when using a 50 kΩ input pulldown resistor. Input power for a logic 1 level (-0.9 volts) on the input is:

$$P_{in1} = \frac{(V_{EE} - \text{logic 1})^2}{R_P} = 0.37 \text{ mW}.$$

Input power for a logic ∅ (-1.7 volts) on the input is:

$$P_{in\emptyset} = \frac{(V_{EE} - \text{logic } \emptyset)^2}{R_P} = 0.25 \text{ mW}.$$

Totaling the input and gate power gives a typical 26.4 mW power per gate for a dual four-input gate, with two inputs high on each gate.

Output power is a function of the load network. It is usually computed for circuits operating at a 50% duty cycle by calculating the 1 and ∅ level output powers and forming their average.

Figure 5-3 shows output transistor powers and load resistor powers for several of the popular terminations. This power must be added to gate power when determining system power. Unused outputs draw no power and may be ignored.

5-3: Typical Output Power

TERMINATING RESISTOR	P Q7 or Q8 (mW)	P RESISTOR (mW)	P TOTAL (mW)
150 ohms to -2.0 Vdc	5.0	4.3	9.3
100 ohms to -2.0 Vdc	7.5	6.5	14
75 ohms to -2.0 Vdc	10	8.7	18.7
50 ohms to -2.0 Vdc	15	13	28
2.0 k ohms to V_{EE}	2.5	7.7	10.2
1.0 k ohm to V_{EE}	4.9	15.4	20.3
680 ohms to V_{EE}	7.2	22.6	29.8
510 ohms to V_{EE}	9.7	30.2	39.9
270 ohms to V_{EE}	18.3	57.2	75.5
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140	165

Calculations for power required with an external 510 Ω output pulldown resistor are:

$$I_R \text{ (logic 1)} = \frac{V_{EE} - \text{logic 1 level}}{R_P \text{ (output)}} = -8.43 \text{ mA}.$$

So: $P_{Q7 \text{ or } Q8} = (I_R \text{ logic 1})(\text{logic 1 level}) = (-8.43)(-0.9) = 7.6 \text{ mW}$

(Q7 or Q8, depending upon which is connected to the 510 Ω output pulldown);

and: $P_{510 \text{ ohm}} = (I_R \text{ logic 1})(V_{EE} - \text{logic 1 level}) = 36.3 \text{ mW}.$

Similar calculations for a logic ∅ state give $P_{Q7 \text{ or } Q8} = 11.7$ mW and $P_{510 \text{ ohm}} = 24$ mW. Averaging ∅ and 1 level powers, gives:

$$P_{510\Omega} = 30.2 \text{ mW avg.;}$$

$$P_{Q7 \text{ or } Q8} = 9.7 \text{ mW avg.}$$

Low impedance MECL III circuits require more input power because of their 2 kΩ input resistors. An average of 7.7 mW per used input must be added to the power for the rest of the circuit:

$$P_{in1} = \frac{(V_{EE} - \text{logic 1 level})^2}{R_{in}} = 9.3 \text{ mW ;}$$

$$P_{in\emptyset} = \frac{(V_{EE} - \text{logic } \emptyset \text{ level})^2}{R_{in}} = 6.1 \text{ mW .}$$

MECL II normally uses internal output pulldown resistors. Power in these resistors is part of the gate specification, so no addition of an output power figure is needed.

Power Supply Considerations

The loose ±10% power supply regulation specification for MECL circuits gives the designer some freedom with operating voltage. If greater than the nominal -5.2 volt supply is used there is an increase in noise margin due to the larger signal swing. The cost is increased power dissipation. Circuit speed is optimized at -5.2 volts but there is a negligible loss of performance over a ±5% voltage range.

Power supply output impedance requirements are dependent on the MECL family used. MECL II, without transmission lines, has very low switching current (less than 100 μA per input) in the signal line and only a 740 μA current differential (in the 1.5 kΩ pulldown resistor) between logic 1 and ∅ levels. This low current difference between logic states, along with complementary outputs on many gates and flip-flops, makes power supply drain essentially constant – independent of logic state and speed of operation. Power supply requirements are therefore not stringent. Simple bridge rectifiers with capacitor filters have been used on small MECL II systems. Larger systems with increased current drain require regulated supplies.

MECL 10,000, used without transmission lines, requires slightly more switching current (less than 2.0 mA) because of its smaller pull down resistors (typically 510 Ω) and lower input impedance. Even so, worst case fluctuation in current requirements is less than 12 percent. In system use the fluctuation would normally be much less than 12% because of complementary outputs and the low probability of all circuits being in a logic 1 or ∅ state at the same time.

Power supply requirements do become more important for MECL 10,000 and MECL III when they are used with transmission lines. In particular, a 50 ohm parallel terminated transmission line sinks 22 mA with a logic 1 output, and 6 mA with a logic ∅. The 16 mA differential between the two states can produce a

significant power supply current fluctuation. Such an effect should be considered when specifying the power supply.

The current fluctuations are by no means insurmountable. Brief current changes are smoothed by bypass capacitors at the circuits. However longer current changes could cause noise on the supply lines unless a properly regulated supply is used. Fortunately, the presence of complementary outputs and the typical 50% distribution of output logic levels minimize current changes.

High frequency noise and ripple from the power supply should be avoided because they produce, in effect, differences in voltage levels among sections of a system, and lead to loss of noise margin. As a rule of thumb, noise can be considered "high frequency" whenever the mean wave length of the noise on the power lines is *not* several times greater than the length of the longest power line. It is recommended that for operation with MECL, high frequency supply noise be held to under 50 mV.

When multiple power supplies are used, the positive terminals should be connected together with a large bus and the output voltages maintained as equal as possible. It is desirable to keep the various supply levels within 50 mV of one another.

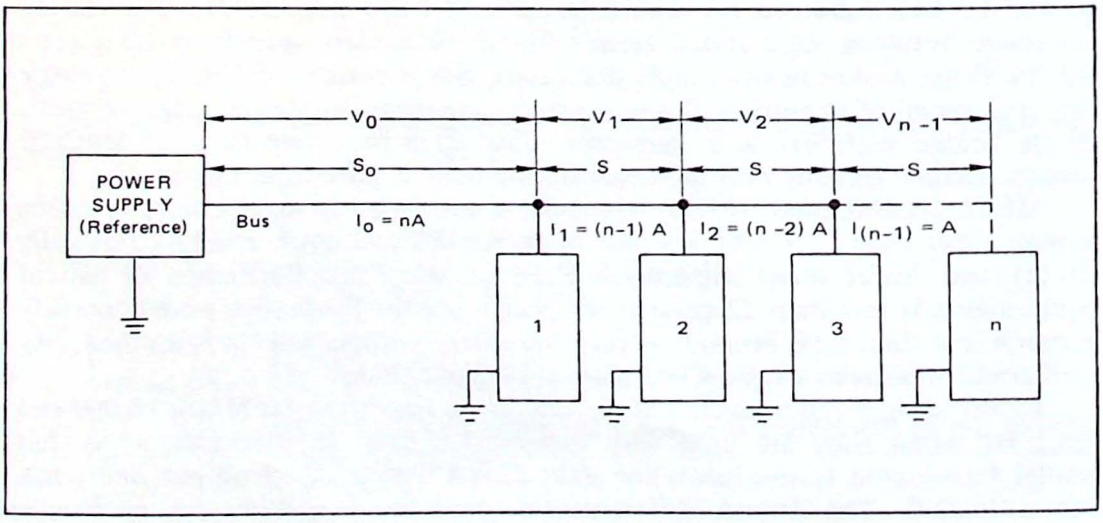
System Power Distribution

When designing the system power distribution network, primary areas of concern are:

1. Maintaining a low impedance ground – without voltage drops;
2. Limiting V_{EE} voltage drops;
3. Designing the supply lines to hinder external noise from coupling into the system.

The following method is used to calculate voltage drops along a voltage bus which has distributed loads (cf Figure 5-4).

5-4: Voltage Drops Along a Power Bus



Where:

S = average spacing of cards in inches,
r = resistance per inch of bus (ohms/in),
n = number of cards,
A = average card current load (amps),
and S_o = distance from reference to first card (inches),

the voltage drop to the first card will be:

$$V_o = I \cdot R = (n \cdot A)(S_o \cdot r).$$

Between cards 1 and 2 the voltage drop is:

$$V_1 = (n - 1)A \cdot (S \cdot r).$$

Likewise:

$$V_2 = (n - 2)A \cdot (S \cdot r),$$
$$V_3 = \text{etc.}$$

So:

$$V'_n = n A S_o r + \sum_{1}^{n} V_n$$

$$= n A S_o r + A S r \sum_{1}^{n-1} n .$$

Example:

let $S_o = 5$ inches, $S = 1$ inch,
$r = 0.0004$ ohms/inch, $A = 500$ mA,
$n = 10$.

The voltage drop to package 10,

$$V'_{10} = 10^{-2} + 2 \times 10^{-4} (1 + 2 + 3 + 4 + 5 + 6 + 7 + 8 + 9)$$

$$= 19 \text{ mV}.$$

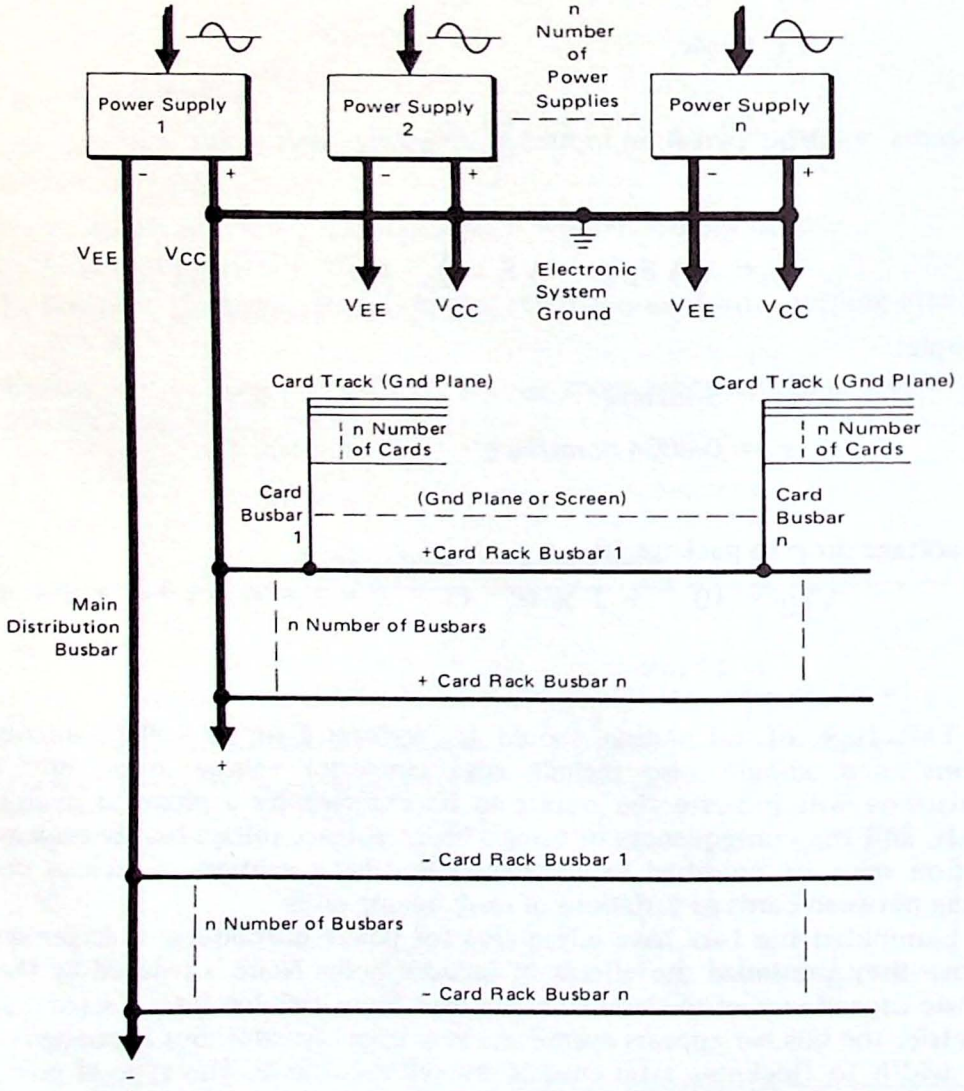
This type of calculation should be performed for all voltage distribution systems, and should also include edge connector voltage drops, etc. These calculations will indicate the results to be expected for a proposed distribution system, and the consequences of using a high resistance voltage bus are evident. The equation may be modified to accommodate other conditions – such as unequal spacing between cards or variations of loads among cards.

Laminated bus bars have advantages for power distribution to larger systems because they minimize the effects of induced noise. Noise is reduced by the high intrinsic capacitance of the laminated bus bars. Since each bus layer is separated by a dielectric, the bus bar appears overall as a very large capacitor. Bus bar design using a large width to thickness ratio ensures low self inductance. This type of power bus system is available with various options from many manufacturers.

For large systems, power distribution should avoid ground loops. Figure 5-5 shows power distribution to a typical large system. The flow of power from the supplies is via main bus bars directly to the ground plane or ground screen of individual card racks and cards. This method minimizes supply losses which would otherwise occur with power supplied through a series string of card racks.

In addition to preventing large voltage drops along the supply lines, the power distribution system must be designed to ward off external noise interference. All noisy and high power devices such as relays and motors should use a separate power supply and ground system. The ground systems are connected at the system ground point which is normally at the power supply. Relays and solenoids should be diode suppressed and motor brushes should be filtered. Other standard design practices should also be used to eliminate these sources of noise.

5-5: Power Supply System



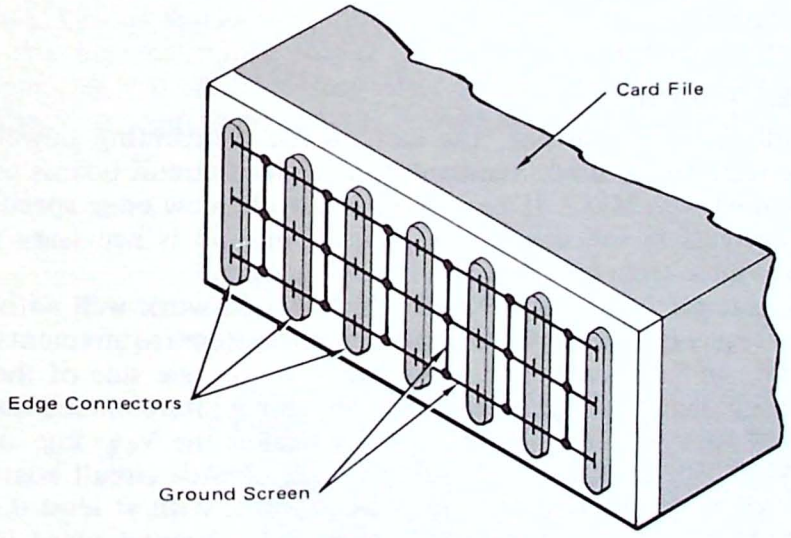
The mechanical sections of a system are commonly connected together with another ground. The frame connecting the panels to the chassis is used for this ground if good electrical conduction is made at points of mechanical contact. This hardware ground is also connected at the common ground point (cf Figure 2-10).

Backplane Power Distribution

For systems using MECL II or MECL 10,000 circuits a common hard wired backplane is often used. The wires are either soldered or wire wrapped to connectors and are routed over a ground plane or ground screen. The ground plane is often formed by a large printed circuit board to which the connectors are mounted, or else, the ground plane is connected to the frame holding the card connectors. The metal is left on one side of the board and forms the ground plane for the backplane wiring. Alternatively, metal can be left on both sides of the board, to conduct both ground and V_{EE}. Ground plane circuit boards are commonly used over a metal ground plane as a means of isolating the MECL circuit ground system from the mechanical system component ground.

When a ground plane is not practical, a ground screen should be constructed on the backplane. A ground screen is made by connecting bus wires (wire size compatible with connector) to the edge connectors in a grid pattern prior to signal wiring, as shown in Figure 5-6. About every sixth pin on the card edge connectors is

5-6: Ground Screen Construction



used as a ground, providing connection points for the ground grid. This interconnection of ground points forms a grid network of approximately 1 inch squares over which the signal lines are wired. A characteristic impedance for a wire over ground screen of about 140 ohms can be expected, depending upon the exact routing and distance from the ground screen. The capacitance of this type line will be about 1 to 2 pF per inch, and series inductance will be about 20 nH per inch.

Point-to-point wiring is normally used instead of routing along channels, to shorten the interconnecting paths and minimize crosstalk which would occur among parallel signal paths. The system interconnecting methods of Chapter 4 are used in backplane wiring over a ground screen.

The faster edges of MECL III require a transmission line environment for connecting among circuit boards. One method is to use coaxial cable for interconnections, and matched impedance connectors on the boards. Care must be taken when stubbing off the cable using a connector "T", because of the short stub length allowed with MECL III. Normally this is avoided in favor of wiring with a single output per cable.

MECL III works very well with twisted pair lines if these lines are specified to have a constant, defined impedance. Differentially driven twisted pair lines with an MC1692 line receiver should always be used where there may be significant power supply voltage drops or noise on the ground system. The board connectors used with the twisted pair lines should be designed to minimize reflection from the interconnect point. Standard edge connectors with the terminating resistor and line receiver close to the point where the line meets the connector (within 1 inch) normally provide adequate termination points.

Although coaxial cable and twisted pair line do not require a ground plane in the backplane for impedance matching, the ground plane must be retained in both cases for a good circuit ground.

Multilayer backplane wiring (motherboard) is commonly used with MECL III. Striplines and microstrip line interconnects are designed in the circuit board, along with ground and V_{EE} voltage planes. Matched impedance connectors are available to permit interfacing between cards and the backplane motherboard without line discontinuity. This technique is normally used when a system design is sufficiently determined to minimize changes in the backplane wiring.

On - Card Power Distribution

Just as with backplane wiring, the method for distributing power on cards depends on the logic family used. Standard double sided circuit boards with a good ground may be used with MECL II because of relatively slow edge speeds and very low switching currents in the signal lines. A good ground is necessary to prevent voltage drops and noise from reducing circuit noise margin.

Here's an example of a circuit board which would work well with MECL II. The various techniques can be modified to fit specific system requirements.

The majority of interconnecting wires would be on one side of the board. A ground bus or modified ground plane with any remaining interconnections would be on the other side. The -5.2 Vdc line is not as critical as the V_{CC} line and may be routed as necessary. The ground buses would be made of wide circuit board paths on the card. The width should be kept as large as possible, with at least 0.15 inch of width for each 10 packages recommended. A modified ground plane is made by leaving the metal on one side of the board and etching only as necessary to run the interconnecting leads for devices on the other side. The layout should be planned so that such interconnecting paths will not cut off a section of the ground plane from the ground inputs or isolate a section so that it is connected only with a narrow metal strip to the rest of the ground plane.

For either method, circuit board grounding is simplified if several pins in the edge connector are used for ground. A standard 22 pin connector could have four or five evenly spaced pins on the connector allocated to ground.

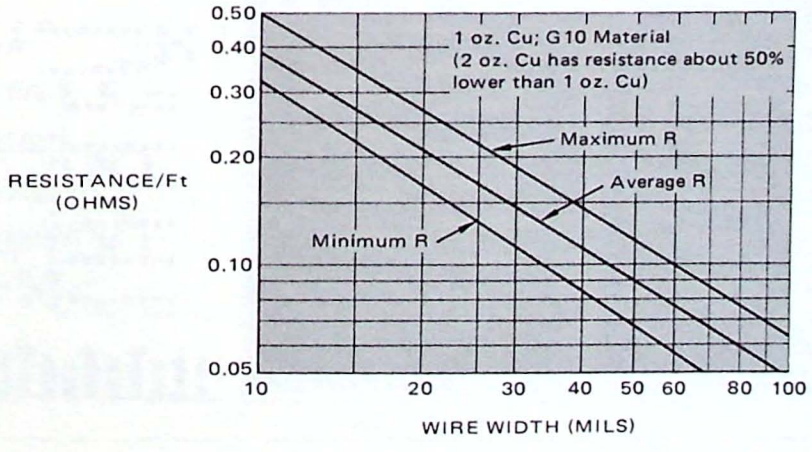
Power supply bypass capacitors are used on the circuit boards to handle the small current transients required by signal lines for charging stray capacitances. Bypass capacitors also lower the supply impedance on the card, reducing noise on the V_{EE} line. Typically a 1 to 10 μF capacitor is placed on the board at the power supply inputs, and a 0.1 to 0.01 μF RF type capacitor is connected between ground and -5.2 Vdc every four or five packages. RF type capacitors are recommended because of their low inductance. Because of their nearly constant current requirements, many MECL II systems are built without using bypass capacitors, and operate perfectly. However, the use of these capacitors will insure cleaner supply lines, especially at top circuit operating speeds.

MECL 10,000 systems use both standard double sided and multilayered circuit boards. However, when using MECL 10,000, the ground plane described previously for MECL II is recommended. Such a ground plane permits low impedance signal lines (over the ground plane) which may be terminated for optimum performance. Also, a ground plane gives the solid ground necessary for suppressing the current transients arising in parallel terminated lines and eliminates possible high frequency ground loops. Ideally, the ground plane would fully cover one side of the circuit board. However with MECL 10,000, ground planes covering greater than 70 percent of the board surface area give good results.

The V_{CC1} and V_{CC2} pins of MECL 10,000 and MECL III packages should be connected directly to the ground plane as closely as possible to the package. V_{CC1} should equal V_{CC2} for best operation. If V_{CC1} drops below V_{CC2} by more than two tenths of a volt, the output devices could saturate and cause additional propagation delays.

When designing the V_{EE} line, care should be taken to prevent excessive voltage drop in the line. Figure 5-7 shows the bus resistance per foot for microstrip lines. This should be taken into consideration when designing large cards with high current requirements. Use of bypass capacitors with MECL 10,000 is strongly recommended to handle the current transients occurring when parallel terminated transmission lines are used. A 1.0 to 10 μF capacitor at the power supply inputs and 0.1 to 0.01 μF capacitors every four or five packages along the board give a low impedance supply.

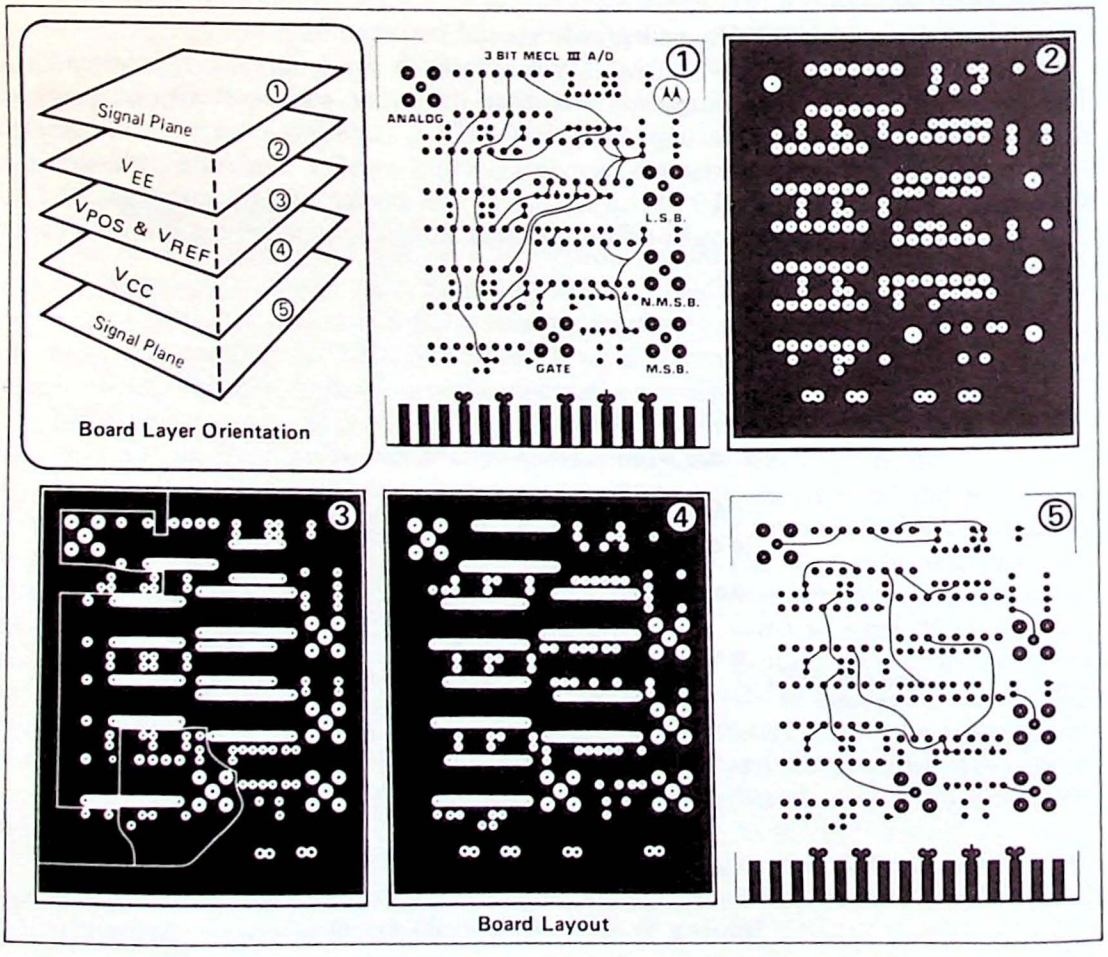
5-7: Bus. Resistance Per Foot for Microstrip Lines



Multilayer circuit boards are ordinarily used with MECL III. For small systems (with few packages) or small test circuits, a double sided board with a good ground plane may be used. With larger systems or systems operating above 200 MHz, multilayer boards are recommended for two reasons: to eliminate ground loops caused by the use of what would normally be ground plane areas as signal paths, and to provide uniform transmission line characteristics. Multilayer boards can be used for other advantages in MECL III systems – possible higher packing density and shorter interconnecting lines.

The layout of a typical small MECL III multilayer board is shown in Figure 5-8. When using multilayer boards, the correct use of ground and voltage planes leads to specific benefits and eliminates serious problems. For instance, when adjacent signal lines are switching, signal line crosstalk may occur. Crosstalk can be reduced by using a voltage plane to separate successive layers of signal lines. Ground lines, between parallel lines on a signal plane, connected to the ground plane via plated-through holes, give additional protection against noise coupling.

5-8: Typical MECL III Multilayer Board Layout



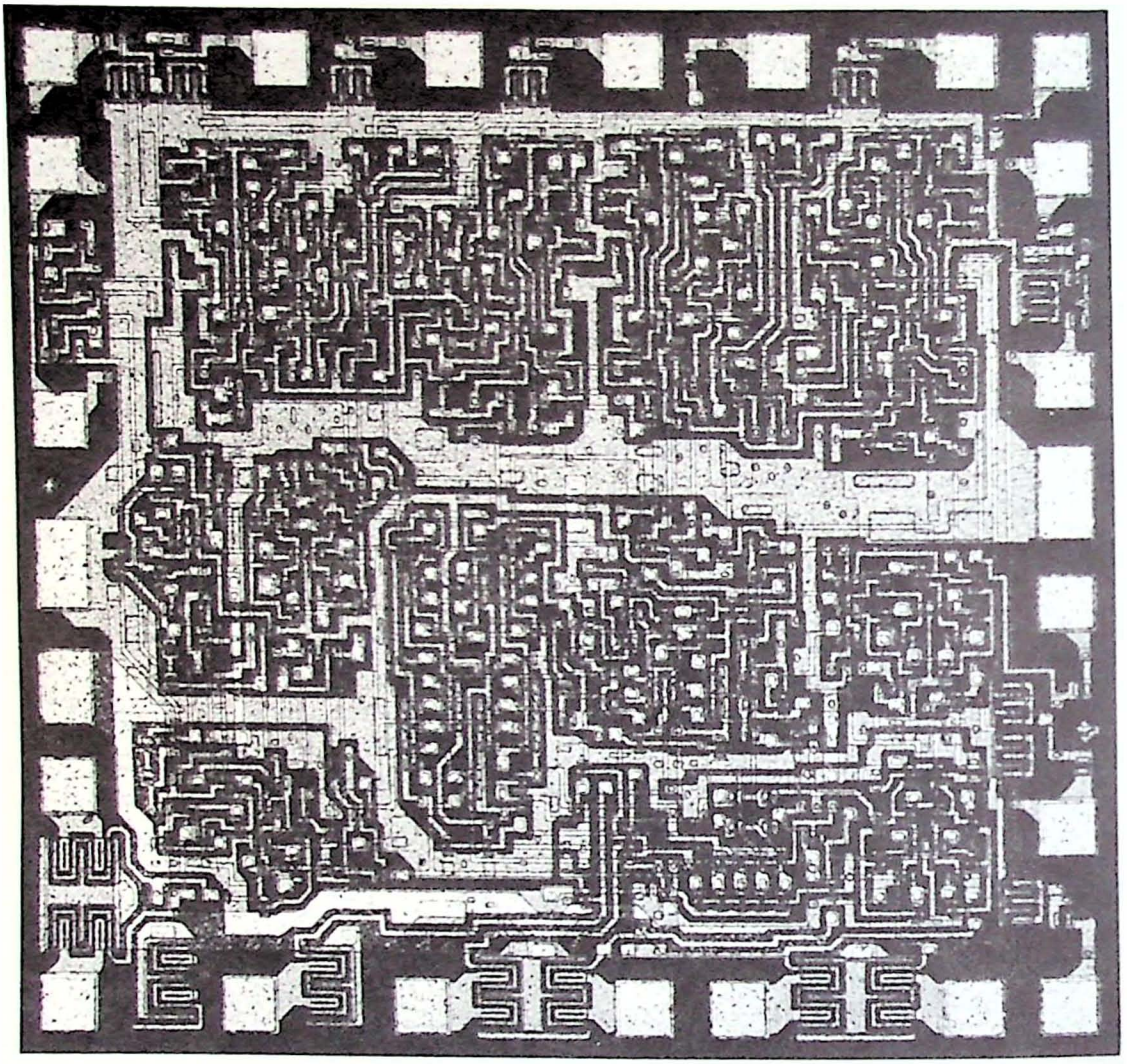
If two successive layers are used for signal interconnects, the use of an orthogonal system is suggested, i.e. interconnects running on one layer are perpendicular to those on the other. This will facilitate layout and reduce crosstalk problems. An associated ground plane can follow below to give ground reference to the two layers of signal lines. V_{EE} may be a separate plane or may be included with one of the signal planes.

The multilayer board ground planes provide a non-inductive, capacitive decoupling function. However, the thickness of the dielectric separating the voltage planes may be too great to provide sufficient inherent low frequency decoupling. In such a case, discrete capacitors are needed. These should be 0.1 to 0.01 μF in value, and are to be placed every three to five packages, to minimize voltage transients between the voltage planes (i.e. ground and V_{EE}).

V_{TT} Termination Voltage Distribution

The generation of a separate -2 Vdc termination voltage, common to all termination resistors, may be advantageous in many system designs. This is an alternate approach to the Thevenin equivalent resistor termination for each parallel termination, in which two resistors are needed.

The decision to use a separate -2 volt supply will depend on the system size. If it is feasible to provide a separate -2 volt supply, then lower termination component count per termination (one less resistor) and a power saving (up to a factor of 4) will be achieved. Since the V_{TT} supply is only used to sink current through the termination resistors, current regulation and ripple are not critical. A good rule to follow is to use the same design practices for V_{TT} as used for the negative supply, V_{EE}. However, if the system is small, cost may weigh against the use of a separate -2 volt supply. Also, the short circuit interconnects of many small systems use only a single pulldown resistor, and this reduces the need for a separate V_{TT} supply.



Complex MECL logic functions are exemplified by this microphotograph of the MC10181 Arithmetic/Logic Unit die. The array is a member of the MECL 10,000 logic family – whose low power gate is permitting a higher level of sophistication in the use of emitter coupled logic. (Some applications for this integrated circuit are discussed in Chapter 8).

CHAPTER 6 Thermal Considerations

The electrical power dissipated in any integrated circuit forms a heat source in the package. This heat source increases the temperature of the circuit die relative to some reference point (normally 25°C ambient) in an amount which depends upon the net thermal resistance between the heat source and the reference point. Thermal resistance, θ, is the difference between the temperature of the junction and the temperature of the reference point, per unit power dissipation. Thermal resistance is the primary figure of merit for the power handling capability of any integrated circuit package. Thermal resistance from "junction to case", θ_{JC}, and/or the thermal resistance from "junction to ambient", θ_{JA}, are the thermal parameters most often specified for integrated circuit packages.

The junction temperature, T_J, for a given junction-to-ambient thermal resistance θ_{JA}, power dissipation P_D, and ambient temperature T_A, is given by:

$$T_J = P_D \theta_{JA} + T_A .$$

If a heat sink with thermal resistance θ_{SA} (sink to ambient) is used and the thermal resistance from junction to case, θ_{JC}, is given, then:

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A,$$

where θ_{CS} is the thermal resistance from the integrated circuit package (case) to the heat sink. Due to the poor thermal conductivity of still air, the factor θ_{CS} may be significant if air voids exist. When using dual in-line MECL III packages that dissipate more than 450 mW, θ_{CS} should be reduced to a usable value by applying a good thermal paste between the package and the sink.

All integrated circuits, including the high speed MECL family members, have maximum allowable junction temperature limits. The MECL II family is specified as having T_J (max) = 150°C in plastic packages and 175°C in ceramic packages; the MECL 10,000 family has T_J (max) = 125°C; and the MECL III family has T_J (max) = 110°C. These limits are generally lower than for most other integrated circuits which may have a T_J (max) of between 175 and 200°C. With very high speed MECL circuits, stray die capacitances must be held to an absolute minimum. To do this, the on-chip interconnect metallization is made narrow. Here the current density and junction temperature become a significant concern to the integrated circuit device designer and require a lower junction temperature limit.

Thermal resistance usually is not specified for digital integrated circuits though maximum power dissipation is generally defined. The maximum ambient temperature rating has been the usual thermal limit of interest to the digital integrated circuit user. The system designer using MECL should be aware of the device junction

temperature, regardless of what his ambient temperature is. The lower the junction temperature of a device, the higher the reliability and consequently the life of the device; thus, system MTBF (mean time between failure) will be increased as junction temperatures are decreased.

MECL Integrated Circuit Heat Transfer

The electrical power dissipated in an integrated circuit is the heat source for thermal purposes. That is, the heat flow in watts equals the power dissipation in watts. The power-dissipating circuit elements are within a very narrow region on the top of the die (diffusion depths for MECL are shallow). The top of the die remains isothermal within a few degrees for MECL power dissipation levels.

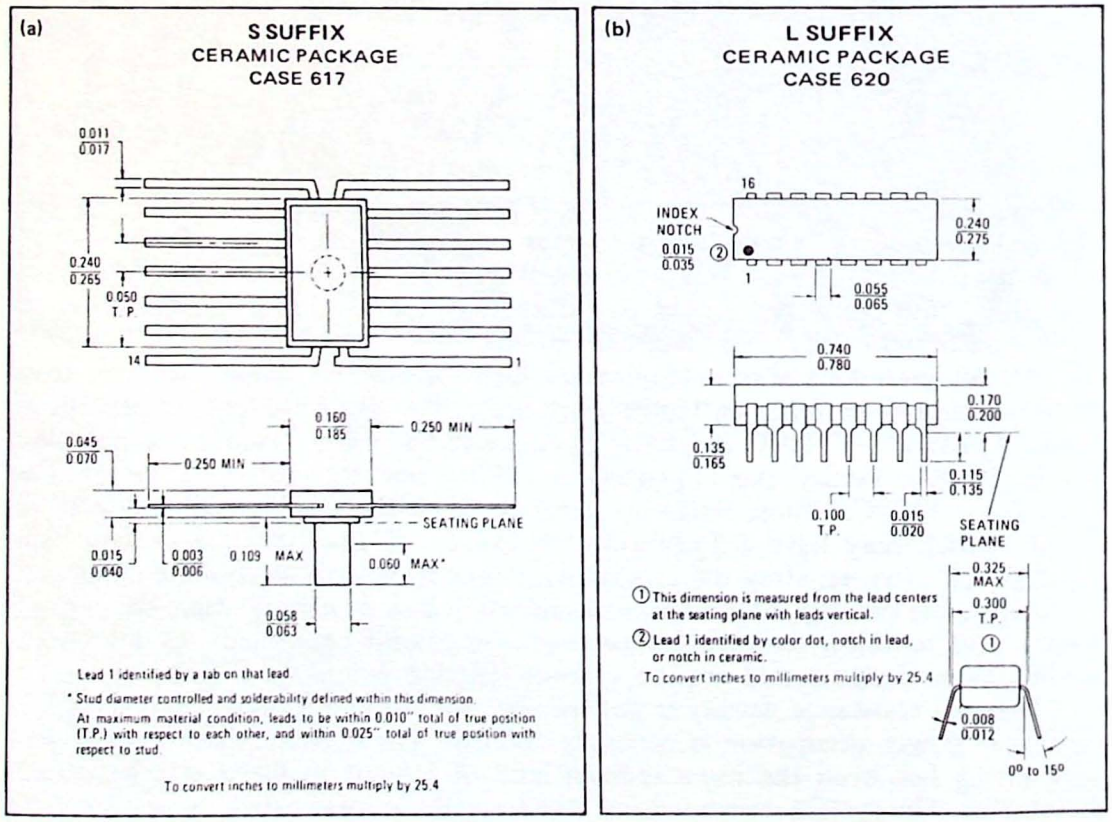
The major means of heat transfer from the top of the die to the outside surfaces of the package is by conduction through solids. Heat transfer through bonding wires from the die to the lead frame is negligible.

Once heat is transmitted to the package, its transfer to ambient depends upon the package mounting technique and its environment. If the integrated circuit package is installed in, or attached to a heat sink, then heat is transferred mainly by conduction to the heat sink, and then by convection and radiation from the heat sink to ambient.

In the 16-pin dual in-line ceramic package (see Figure 6-1b), used for both MECL 10,000 and MECL III, the heat flows from the top of the die, through the

6-1: MECL Package Dimensions

MECL III integrated circuits are available in the 14-lead ceramic flat package with a stud, Case 617 (suffix S), and in the 16-lead dual in-lin ceramic package, Case 620 (suffix L).

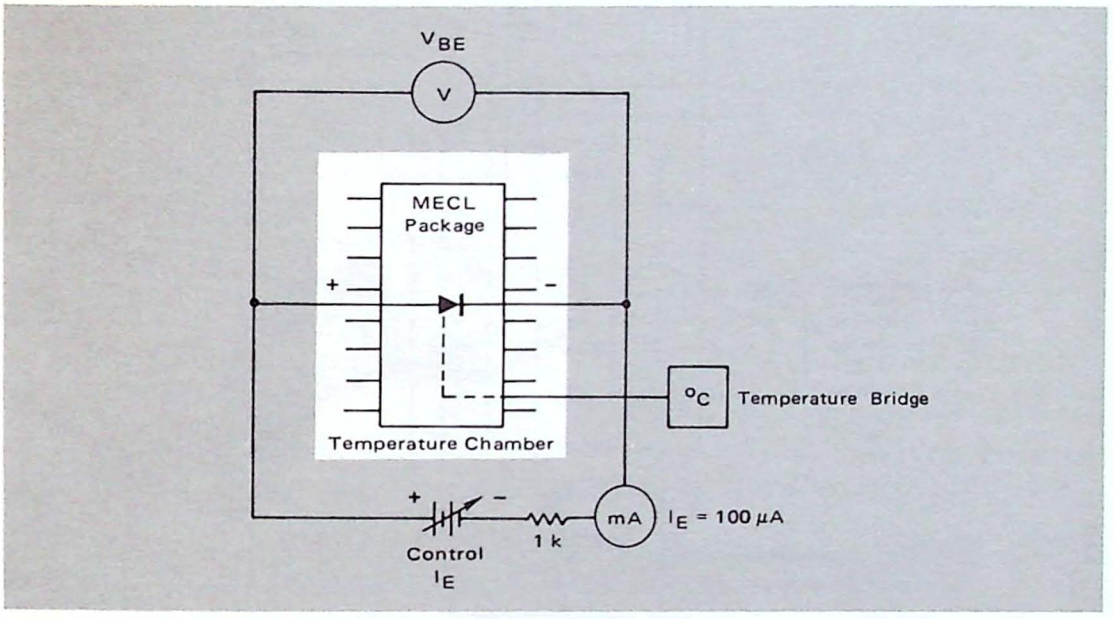


chip and gold eutectic die bond, to the ceramic base. The optimum heat sink location would be in contact with the bottom of the package. Due to the poor thermal conductivity of glass, only a limited amount of heat is transferred from the ceramic base out through the lead frame.

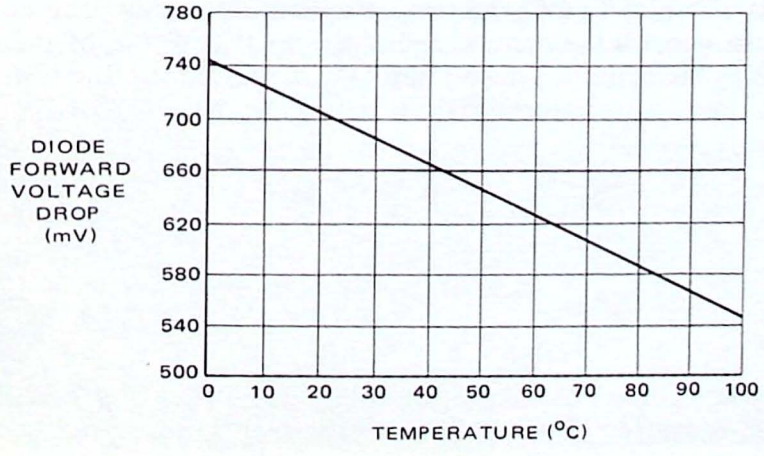
The difference between the temperature of the die and some reference point per unit power dissipation, yields the thermal resistance. The method used to measure the temperature of MECL devices is "internal temperature sensing" – by a special MECL integrated circuit. It employs an independent diode diffused on the chip. It is an easy method to use and calibrate, and has a voltage output that is very nearly a linear function of temperature.

The sensing diode within the MECL package is calibrated as a function of temperature by using the circuit shown in Figure 6-2. The forward V_{BE} drop of the

6-2: Diode Calibration Circuit

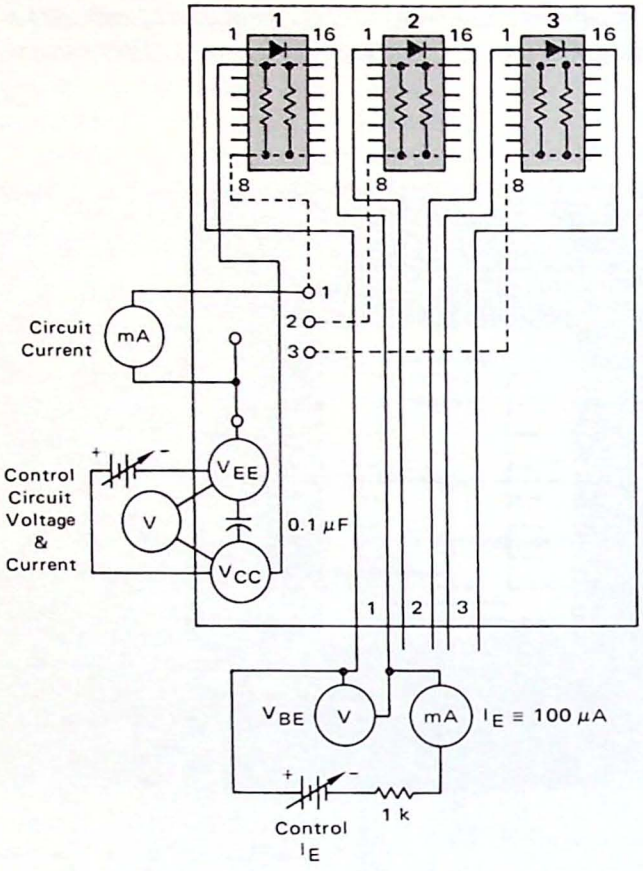


6-3: Typical Thermal Diode Calibration Curve



diode is recorded at stabilized oven temperatures between 0° and 100°C with the diode current held constant at 100 μA. A calibration curve is plotted as shown in Figure 6-3. This curve, along with the data recorded in the test setup of Figure 6-4,

6-4: Thermal Evaluation Test Circuit for 16-Pin Dual In-Line Ceramic Package



will produce data to plot T_J (°C), junction temperature, versus true power (watts). The slope of the curve is the thermal resistance, θ_J (°C/Watt), of the MECL case.

By recording the ambient temperature (T_A in °C) during the test, the thermal resistance from junction to ambient (θ_{JA} in °C/W) may be calculated as:

$$\theta_{JA} = T_{JA}/P_D \text{ (°C/W)},$$

where:

$$T_{JA} = T_J - T_A \text{ (°C)}.$$

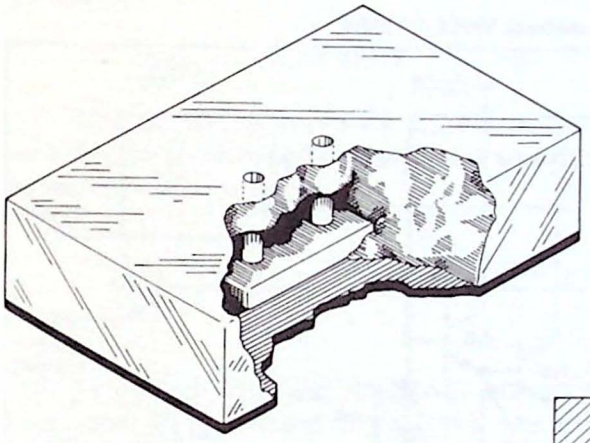
To obtain the thermal resistance from junction to case (θ_{JC}), an infinite heat sink must be provided. This can be approximated by using a copper bar

3-3/4" X 1-1/2" X 1/2" laid in thermal contact with the dual in-line 16-pin ceramic package, or by two 3" X 3" X 1/4" copper planes for the MECL III stud package. Copper-constantin thermocouples should be placed in holes in the sink next to the surface of the package. These thermocouples are used to measure the case temperature. Figure 6-5 shows a sample set-up for an infinite heat sink.

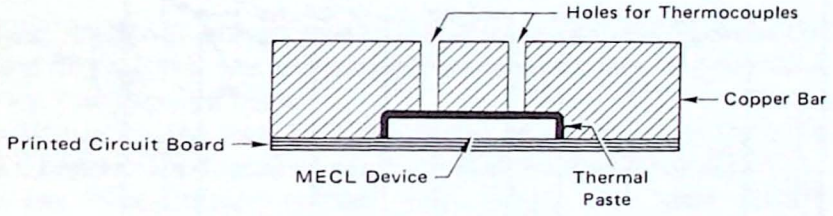
The thermal characteristics of both the 16-pin dual in-line ceramic package and the 14-pin stud flat package, are listed in Figure 6-6. This information is based on the following package characteristics:

(1) 14-pin stud package – ceramic package with molybdenum/gold base; die bond by gold eutectic method. Die well is 0.070 X 0.10 inches. Stud size is 0.105" length X 0.029" diameter.

(2) 16-pin dual in-line package – ceramic black-pigment alumina package with gold/glass-frit base; die bond – gold eutectic; lead frame is 42% nickel, 58% iron, with tin plating; die well is 0.11" X 0.14".



6-5: Sample Infinite Heat Sink



6-6: Typical Thermal Characteristics for MECL Packages

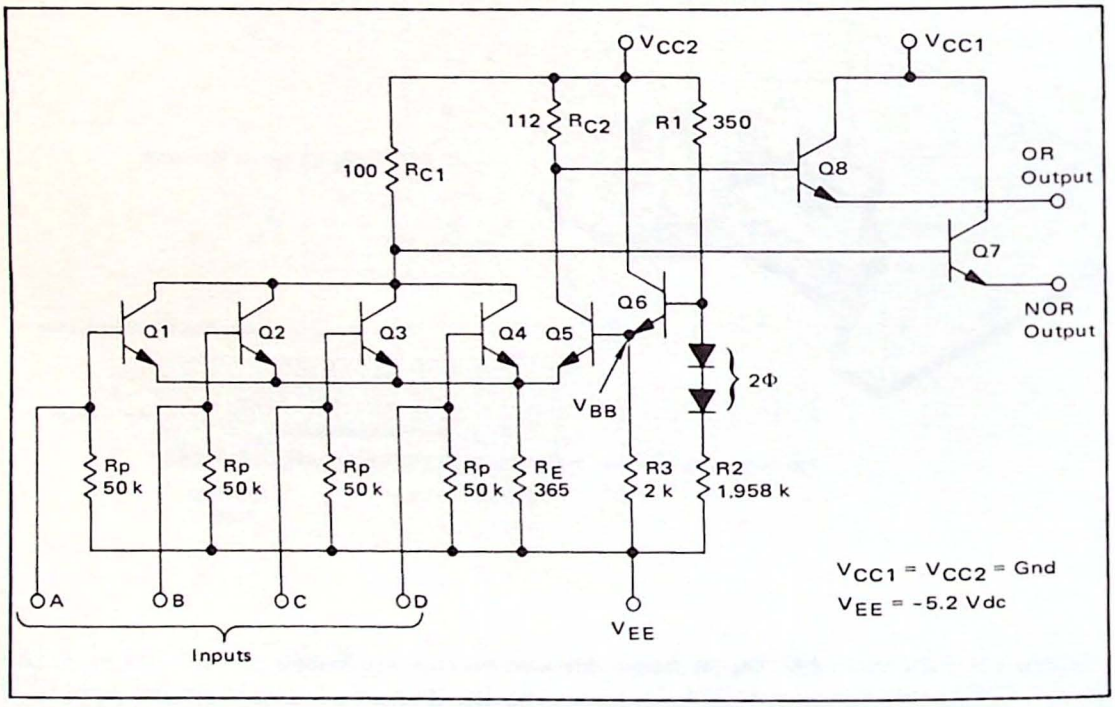
THERMAL CHARACTERISTIC	16-PIN DIP		14-PIN STUD	
	NOTES	TYPICAL VALUE	NOTES	TYPICAL VALUE
θ_{JA}	No heat sink; no air flow; in socket.	85°C/W	V_{EE} stud clip in place; no heat sink	102°C/W
θ_{JA}	No air flow; soldered in 0.062"x6"x4" PC board.	75°C/W	Copper heat sink 0.04"x2"x4"	37°C/W
θ_{JC}	No air flow; mounted in 0.062" 2-5/8"x4" PC board.	25°C/W	Junction to stud	11°C/W

MECL DC Thermal Characteristics

To fully understand the thermal effects on the characteristics of MECL circuits, an explanation of the output level tracking and the reference (V_{BB}) tracking will be presented. Some of the thermal equations offered are used mainly by an MECL integrated circuit designer, but are presented here to illustrate what parameters are changing and how they change as a function of temperature. Figure 6-7 shows the MECL III gate used for equation derivation. For all calculations, an ambient reference temperature of 25°C was chosen. The MECL circuit has the following basic parameters which influence dc performance: V_{BE}, beta, and resistor variations with temperature.

The threshold voltage level (V_{BB}) is most important and so an expression for V_{BB} as a function of V_{BE}, beta, and resistor values in the bias supply is derived first. Then, to analyze the temperature dependence of V_{BB}, a total derivative with respect to temperature is found in terms of dV_{BE}/dT, $d\beta/dT$, dR_1/dT, dR_2/dT, and dR_3/dT.

6-7: Basic High Input Impedance MECL III Gate



If loop equations are written for the bias supply, the expression obtained for V_{BB} is:

$$V_{BB} = \frac{R_1R_3\beta\,(V_{EE} - V_{BE} + 2\Phi) + R_1R_3\,(V_{EE} - V_{BE} + 2\Phi) - \beta\,(R_1R_3 + R_2R_3) + R_2R_3\beta V_{BE} - R_2R_3V_{BE} + R_1R_2V_{EE}}{R_1R_2 + R_2R_3 + R_1R_3} \quad (1)$$

Differentiating with respect to temperature, T:

$$\frac{dV_{BB}}{dT} = \frac{\partial V_{BB}}{\partial R_1}\frac{dR_1}{dT} + \frac{\partial V_{BB}}{\partial R_2}\frac{dR_2}{dT} + \frac{\partial V_{BB}}{\partial V_{BE}}\frac{dV_{BE}}{dT} + \frac{\partial V_{BB}}{\partial R_3}\frac{dR_3}{dT} + \frac{\partial V_{BB}}{\partial \beta}\frac{d\beta}{dT} \tag{2}$$

Solving equation (1) for V_{BB} at 25°C using the parameters,

$R_1 = 0.35\ k\Omega$ $\quad$ $V_{EE} = -5.2$ volts

$R_2 = 1.958\ k\Omega$ $\quad$ $\beta = 100$

$R_3 = 3.0\ k\Omega$ $\quad$ $V_{BE} = 0.745$ volts

$\Phi = 0.80$ volts (junction drop)

we obtain:

$$V_{BB} = -1.29 \text{ volts.} \tag{3}$$

The partial differential equations for reducing equation (2) will not be solved here due to their length. However a solution of (2) will show that the change of V_{BB} with temperature is:

$$dV_{BB}/dT = +1.11\ mV/°C\ . \tag{4}$$

This threshold tracking level will always insure that V_{BB} is centered between the V_{OH} and V_{OL} output logic levels. As a result, noise immunity can be guaranteed across the full operating temperature range.

Temperature variations in the two logic levels can be derived from the basic equations for the MECL gate. The logic 1 level equation is simply a relation of V_{OH} to the emitter-follower base-emitter voltage drop (V_{BE}) plus some further dependence upon emitter-follower base current through the current-switch collector resistor. It can be shown that the contribution by changes in β_{EF} and R_C to the 1 logic level output is about 100 μV/°C. These changes subtract from the nominal dV_{BE}/dT of -1.5 mV/°C.

The basic equation for the 1 logic level is:

$$V_{OH} = -V_{BE} - I_C R_C\ . \tag{5}$$

Differentiating with respect to temperature and inserting the values discussed:

$$\frac{dV_{OH}}{dT} = (-1)(-1.5\ mV/°C) - 0.1\ mV/°C \tag{6}$$

$$\frac{dV_{OH}}{dT} = +1.5\ mV/°C - 0.1\ mV/°C = +1.4\ mV/°C\ . \tag{7}$$

∅ Level Dependence on Temperature

The logic ∅ level can be calculated by developing the following equation from Figure 6-7:

$$V_{OL\,(OR)} = -\left[\frac{-\left(\frac{-V_{EE} - 2\Phi}{R_1 + R_2}\right)R_1 - V_{BE1} - V_{BE2} - V_{EE}}{R_E}\right] R_{C2} - V_{BE3}, \tag{8}$$

where:

V_{EE} = -5.2 volts,

V_{BE1} = 0.745 volts (bias driver transistor),

V_{BE2} = 0.870 volts (current switch transistor),

V_{BE3} = 0.810 volts (emitter-follower transistor),

Φ = 0.800 volts (bias driver diode drop).

Substituting values yields:

$$V_{OL\,(OR)} = -1.745 \text{ volts.} \tag{9}$$

The logic zero level change with temperature can now be calculated from:

$$\frac{dV_{OL\,(OR)}}{dT} = \left\{\left[\frac{\left(2 - \frac{2R_1}{R_1 + R_2}\right)}{R_E}\right] R_{C2} - 1\right\} \frac{dV_{BE}}{dT}. \tag{10}$$

So,

$$\frac{dV_{OL\,(OR)}}{dT} = (0.514)\,(-1.5 \text{ mV/°C}) = 0.771 \text{ mV/°C}.$$

In normal operating temperature environments, the bias voltage shifts in such a way that it always remains halfway between the logic levels. Figure 6-8 shows the logic levels as a function of temperature for the MECL III gate.

The effects of temperature on MECL can be illustrated by a specific example. Assume that within a panel, one card is operating near the inlet airflow duct at 25°C, and another interconnected card (remote from the air inlet) is at 35°C. Thus a 10°C thermal differential exists within the system. The 25°C device has a typical V_{OH} of -0.900 volts and a V_{OL} of -1.700 volts. The 35°C device will have the following typical levels:

$$V_{OH}\,(35°C) = V_{OH}\,(25\,°C) + \frac{dV_{OH}}{dT}\,(\Delta T)$$

$$V_{OH}\,(35°C) = (-900\ \text{mV}) + (1.4\ \text{mV/°C})\,(10°C) = -0.886\ \text{volts.}$$

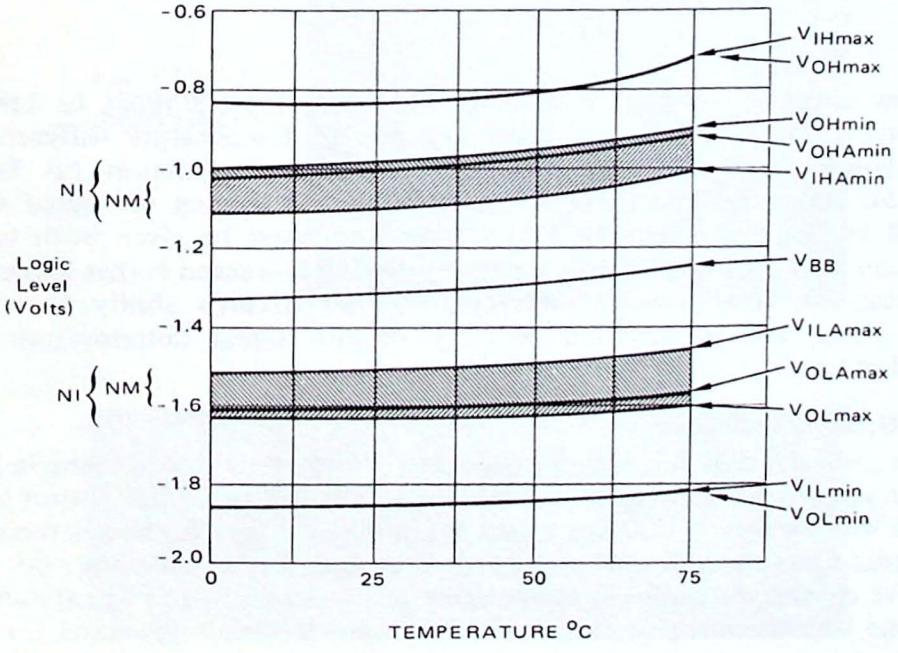
$$V_{OL}\,(35°C) = V_{OL}\,(25\,°C) + \frac{dV_{OL}}{dT}\,(\Delta T)$$

$$V_{OL}\,(35°C) = (-1{,}700\ \text{mV}) + (0.77\ \text{mV/°C})\,(10°C) = -1.692\ \text{volts.}$$

This shows that a shift of only 14 mV took place in the logic 1 level and about 8 mV in the logic Ø level. The overall loss in noise immunity (N.I.) would be even smaller than these figures – due to the positive threshold-shift. It is recommended that thermal gradients be limited to on-card differentials under 35°C. If differentials on a card get as great or greater than 35°C, then good thermal management has not been employed. However when a differential of 35°C or greater exists between panels or cabinets, another feature of MECL logic can be used to advantage: namely, the availability of complementary output devices and line receivers allows a differential mode of line driving and receiving which eliminates the loss of noise immunity between units that have large temperature differences. The differential transmission of signals on twisted pair is covered in detail in Chapter 4.

The measure of safety, noise margin (N.M.), is defined as the worst case input threshold voltage (V_{IHA}(min) or V_{ILA}(max)) for which the output is still within specified limits ($>V_{OLA}$ or $<V_{OHA}$), as was indicated in Chapter 1.

6-8: MECL III Logic Levels versus Temperature



That is:

$$\text{N.M. (logic } \emptyset \text{ level)} = V_{ILA}(\max) - V_{OLA}(\max)$$

$$\text{N.M. (logic 1 level)} = V_{OHA}(\min) - V_{IHA}(\min).$$

As can be seen from the data in Figure 6-9, a worst case noise margin of 125 mV is guaranteed for the stud package, and a worst case noise margin of 115 mV is guaranteed for the dual in-line 16-pin ceramic package (both between 0 and 75°C with packages at the same ambient temperature, T_A). The majority of the 10 mV N.M. difference between the flat and the DIP packages can be attributed to differences in package thermal resistances. For MECL 10,000, worst case noise margin is 125 mV, while MECL II is specified at 175 mV.

6-9: MECL III Worst-Case Logic Levels

VOLTAGE LEVEL (VOLTS)	ENVIRONMENT TEMPERATURE					
	S-PACKAGE			L-PACKAGE		
	0°C	25°C	75°C	0°C	25°C	75°C
$V_{IH(max)}$	-0.820	-0.790	-0.700	-0.840	-0.810	-0.720
$V_{OH(max)}$	-0.850	-0.820	-0.730	-0.840	-0.810	-0.720
$V_{OH(min)}$	-0.995	-0.950	-0.895	-1.000	-0.960	-0.900
$V_{IL(min)}$	-1.870	-1.850	-1.830	-1.870	-1.850	-1.830
$V_{OL(min)}$	-1.870	-1.850	-1.830	-1.870	-1.850	-1.830
$V_{OL(max)}$	-1.650	-1.650	-1.630	-1.635	-1.620	-1.595
$V_{OHA(min)}$	-1.015	-1.000	-0.915	-1.020	-0.980	-0.920
$V_{OLA(max)}$	-1.625	-1.600	-1.595	-1.615	-1.600	-1.575
$V_{IHA(min)}$	-1.140	-1.125	-1.040	-1.135	-1.095	-1.035
$V_{ILA(max)}$	-1.500	-1.475	-1.470	-1.500	-1.485	-1.460

NOTE: Output Load R_L is 50 ohms to -2.0 volts.
θ_{JA} equal to 50°C/W.

When calculating system noise immunity three factors must be taken into consideration. These are: loss of immunity due to temperature differentials (as above); power supply line losses, and power supply regulation (as shown in Chapter 5); and signal losses due to undershoot and ringing on signal lines (as described in Chapters 3 and 4). Proper attention must be given both to power distribution and to thermal factors for any system. The reason is that losses derived from these two areas directly subtract from the circuit's ability to withstand external noise, and to function properly despite signal deterioration due to mismatched lines.

Heat Dissipation Techniques

The majority of MECL users provide some form of air flow cooling in medium and large size systems. For this reason MECL 10,000 and MECL III output levels are specified with air flow at 500 linear feet per minute (or greater) across the package. Many small systems and test circuits do not use forced air flow, but do use convective cooling with ambient temperature air, or some form of heat conduction – to avoid large thermal gradients. MECL II output levels are specified for still air,

but many MECL II systems have used forced air cooling to limit air temperatures and thermal differences between packages.

As air passes over devices on a printed circuit board, it absorbs heat from each package. Thus the ambient temperature of the air will increase as it flows from inlet to outlet. The heat gradient from the first package to the last package is a function of the package density, air flow rate, and the individual package dissipations. The table in Figure 6-10 lists this gradient at various power levels for an air flow rate of 500 LFPM. These figures show the increase in junction temperature for each of the 16-pin DIPs as the inlet air passes over each device. Although Z-axis air flow information is given, the figures are similar for air flow 90° from this axis, in the plane of the PC board.

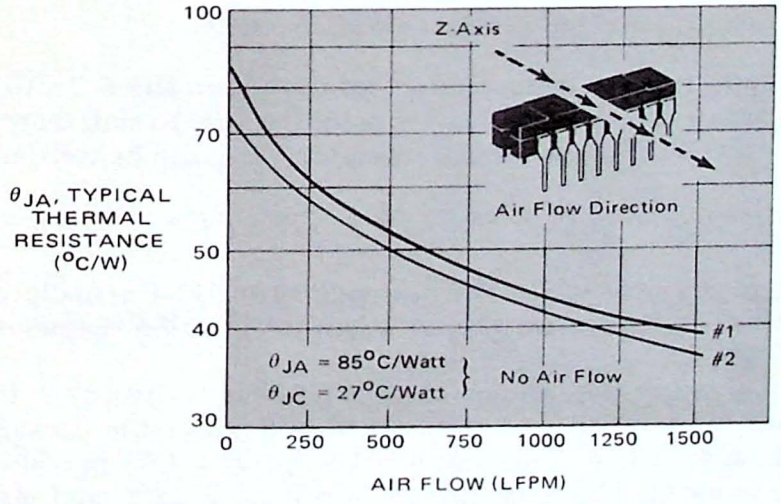
16-PIN DIP POWER DISSIPATION (mW)	T_J GRADIENT (°C/PACKAGE)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062" PC board with Z axis spacing of 0.5" Air flow is 500 LFPM in the Z axis.

6-10: Junction Temperature Thermal Gradients

From the air flow curve of Figure 6-11, the 16-pin ceramic DIP has a θ_{JA} of 50°C/W (MC1660L dual 4 OR/NOR, loaded 50 ohms to -2 Vdc, mounted on

6-11: Typical Thermal Resistance versus Air Flow



Die Size – 0.040"x0.060"
Package Type – 16-Lead Black Ceramic
Dissipation Level – 200 mW
Air Flow – Z-Axis 25°C
Measurement Method – Calibrated Diode
Package Mounting: #1 Barnes Socket (Or Equivalent)
#2 Printed Circuit Board
4"x6"x0.062" – 2 Oz. Cu.

printed circuit board with 500 LFPM air flow). This is a fairly standard air flow rate for cooling a moderate size system. In this case the first device in the 25°C air flow stream would have a junction temperature of:

$$T_J = \theta_{JA} P_D + T_A$$

$$T_J = (50°C/W)\,(0.185\ W) + 25°C = 34.2°C.$$

At an average power level of 200 mW/package, the heat gradient for junction temperature increase is 0.4°C per package. For example, the tenth package in an air flow path would have a junction temperature of 37.8°C.

The following is a typical thermal calculation for the amount of heat sinking to use with a dual in-line ceramic 16-pin MECL III counter circuit dissipating 900 mW. The maximum allowable junction temperature. T_J, is 110°C and the operating ambient temperature, T_A, is 25°C. These calculations are based on still air:

$$\theta_{JA\ max} = \frac{T_{J\ max} - T_{A\ max}}{P_{D\ max}} = \frac{110°C - 25°C}{0.9\ watt} = 94.5°C/watt.$$

It is known that:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA},$$

where: θ_{JC} = thermal resistance, junction to case,

θ_{CS} = thermal resistance, case to heat sink,

θ_{SA} = thermal resistance, sink to ambient;

therefore,

$$\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS}).$$

In still air, the thermal resistance, θ_{JC}, for the 16-pin DIL is 25°C/W. If thermal paste (Dow Corning 340, or equivalent) is used, the case to sink thermal resistance, θ_{CS}, would be 8°C/W. Thus the thermal resistance, θ_{SA}, can be calculated:

$$\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS}) = 94.5°C/W - (25°C/W + 8°C/W) = 61.5°C/W.$$

This is a worst allowable value. The heat sinking method actually chosen should have less thermal resistance than this, to insure the junction temperature (T_J) does not exceed 110°C.

The above calculations assume all package heat is dissipated through a heat sink. However, from Figure 6-11 it is seen that θ_{JA} for the package on a circuit board in still air is 75°C/W. Since this is below the 94.5°C/W previously calculated, it is possible to use the MECL III counter in still air at 25°C and maintain the die temperatures within rated limits.

However, to allow for increased ambient temperatures and tight packaging, it is recommended that MECL III systems be designed *with* air flow, and that high dissipation MSI parts have additional heat sinking.

Mounting Techniques

Mounting techniques are particularly important with MECL III because of its higher package power dissipation. Some of the more complex MSI MECL III

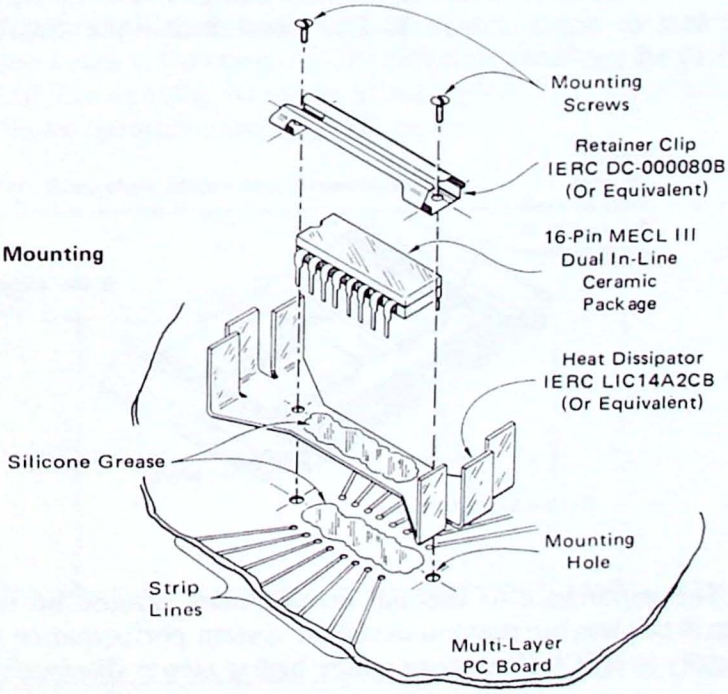
functions, such as the MC1678 decade counter, dissipate up to 900 mW and *do* require special cooling. MECL II and MECL 10,000 dissipate much less package power, so standard mounting is normally more than adequate for most systems. For this reason, most of the mounting techniques discussed in this section apply primarily to MECL III.

The main concern when designing component mounting is to provide not only a good circuit ground path, but also to provide a conductive thermal path away from the package case. The MECL stud flat package presents a problem since the stud, like the collector on some power transistors, is not at ground potential. This means that methods must be used to electrically insulate the stud from ground, while providing a good thermal path to the heat sinking medium.

The use of a multilayer printed circuit layout is the easiest way to provide both a ground plane and a solid thermal path on the V_{EE} (−5.2 volt) plane. Previous discussions about strip lines (cf Chapter 3), have pointed out that a solid ground with no discontinuities is desirable below every microstrip line. Thus it is recommended that the V_{EE} plane (thermal plane) be the bottom layer of the multilayer board, and that 3 ounce copper be used to conduct heat from the stud. However, if the number of MECL III devices used per board is less than 6 packages, then the normal 1- or 2-ounce copper clad may be used.

Two sided printed circuit boards may be used on layouts where the board dimensions and the package count are small. Here the most difficult problem is to maintain a good ground environment between interconnecting signal points. In the two sided layout, where signal lines may have to be placed on both sides of the board, the V_{EE} thermal plane can be used as a pseudo ground plane. This pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane, thus maintaining a microstrip signal line environment.

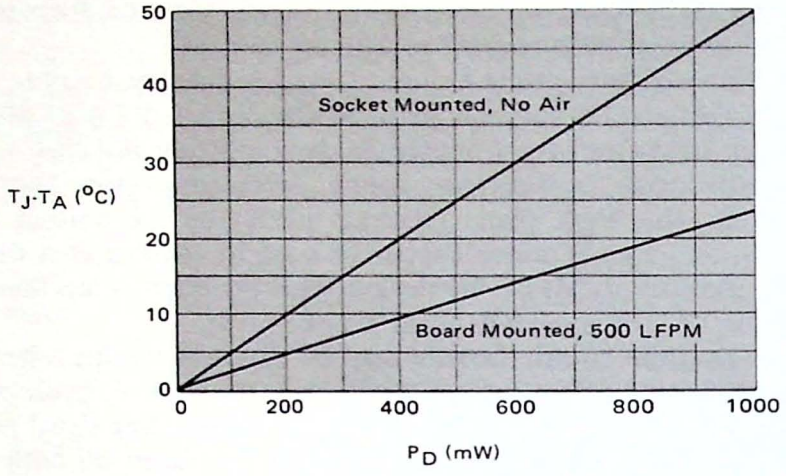
A commercially available heat sink that was developed for use with the 16-pin dual in-line ceramic MECL III package is illustrated in Figure 6-12. This heat sink is



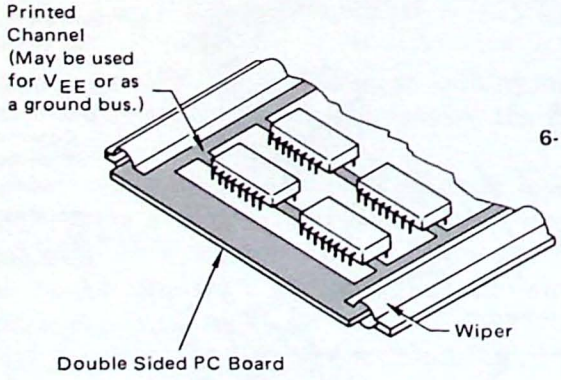
6-12: 16 Pin DIP Heat Sink Mounting

small in size and will not affect lead interconnections. The overall package is very efficient in removing heat from the case as indicated by the graph in Figure 6-13. This type sink is recommended for the MC1678L decade counter complex function, or for that matter, any dual in-line package dissipating ≥ 500 mW. Another suitable heat sink is made by the Thermalloy Corporation.

6-13: Thermal Curves for 16-Pin DIP Heat Sink IERC-LIC 14A2CB (Or Equivalent)



Printed channeling is a useful technique for conducting heat away from the MECL DIP package when the device is soldered into a printed circuit board and thermal paste is used between the package and channel. As illustrated in Figure 6-14, this heat dissipation surface could also serve as a V_{EE} voltage distribution or ground bus. The channels should terminate into channel strips at each side or rear of a plug-in type printed circuit board. Then, by means of wipers that come into thermal contact with the edge channels, the heat can be removed from the circuit board into the cabinet or board slide-rack. This same technique can be used with the MECL stud flat package.



6-14: Channel/Wiper Heat Sinking

The importance of thermal management cannot be overemphasized. Proper design in this area can result in excellent system performance and increased reliability, especially in MECL III systems where higher power dissipation is encountered.

CHAPTER 7 Transmission Line Theory

Understanding the operation of transmission lines used in conjunction with high speed MECL circuits is necessary in order to be able to completely characterize system operation. While it is not expected that every system interconnection will be fully evaluated by a designer, the information in this chapter will be especially useful for setting up system design rules. This chapter describes transmission lines with respect to both line reflections and propagation delay times. Discussed will be the use of the Time Domain Reflectometer (TDR) for measuring transmission line characteristics.

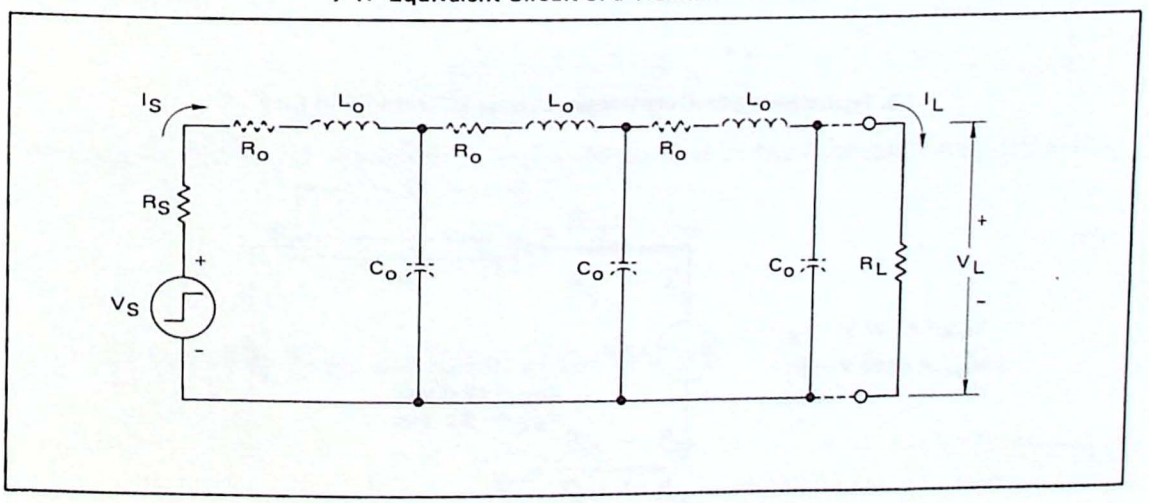
Transmission Line Design Information

A transmission line as used with high speed MECL is a signal path that exhibits a characteristic impedance. Coaxial cables and twisted pair lines have a defined characteristic impedance and are commonly referred to as transmission lines. Equally important, printed circuit fabrication of microstrip and striplines (as discussed in Chapter 3) results in closely-controlled transmission-line impedance.

The equations for voltage and current along a transmission line are fairly universal and may be found in reference 4. These equations show the voltage and current transmitted along a transmission line using the differential equations based on a point along the line.

Transmission lines may be approximated by the lumped constant representation shown in Figure 7-1. The effect of the resistance, R_O, of the line on the characteristic impedance, Z_O, is negligible, but it will cause some loss in voltage at the receiving end of long lines. The inductance and capacitance of the line in the presence of a ground plane are a function of the dielectric medium, the thickness and width of the line, and the spacing from the ground plane. The inductance and capacitance of the line can be measured using an LC meter.

7-1: Equivalent Circuit of a Transmission Line

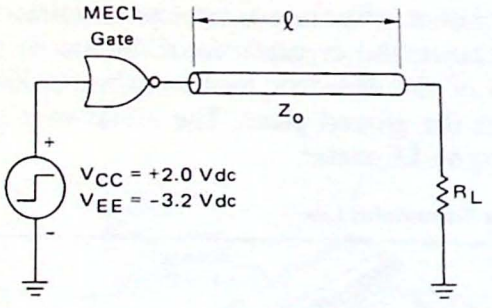


Microstrip and strip lines may be treated as operating in the transverse electro-magnetic (TEM) mode. Although microstrip propagation is not purely TEM because of non-uniform dielectrics, for all practical purposes it can be treated as TEM. The characteristic impedance of the line is $Z_O = \sqrt{L_O/C_O}$ and the propagation delay is $t_{pd} = \sqrt{L_O C_O} = Z_O C_O$. Reference 1 shows that for a homogeneous medium the propagation delay is also equal to $t_{pd} = \sqrt{\mu e} = \sqrt{\mu_O \mu_r e_O e_r}$, where μ is the permeability and e is the permittivity of the medium. In transmission lines, the relative permeability (μ_r) is unity, $\mu_O = 4\pi \times 10^{-7}$ Henry/meter, and $e_O = 8.85 \times 10^{-12}$ Farad/meter. Therefore, $t_{pd} = 1.017 \sqrt{e_r}$ ns/ft, as was discussed earlier in Chapter 3 (e_r is the relative dielectric constant). For microstrip lines on glass epoxy boards $e_r = 3.0$, and for strip lines $e_r = 5.0$ (see reference 1).

From transmission line theory for a lossless line, it can be shown that a signal sent down a line of constant characteristic impedance will travel along the line without distortion. However, when the signal reaches the end of the line, a reflection will occur if the line is not properly terminated with the characteristic impedance of the line.

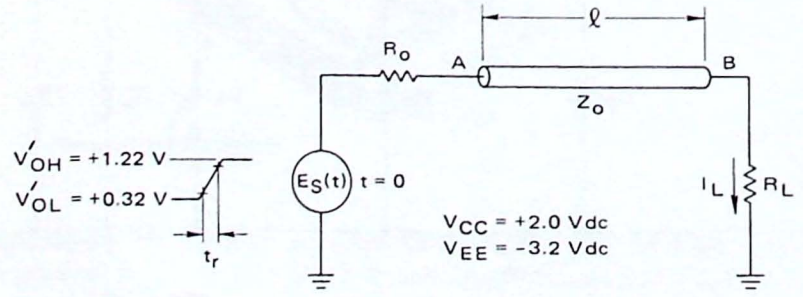
Figure 7-2 shows a MECL gate driving a transmission line terminated in a load resistor, R_L. A negative-going transition on the input to the gate will result in a positive-going transition at the NOR output. The MECL gate is essentially a VHF linear differential amplifier with a bandwidth of $0.37/t_r$ (MHz), where t_r is the rise time of the gate in nanoseconds. The effect of the capacitance of the transmission line will not decrease the bandwidth or affect the rise time at the MECL gate output. However, the signal at the end of a long transmission line may be attenuated due to band width limitations in the particular type of transmission line used. For the purposes of this discussion a long line is defined as a line having a propagation delay larger than the rise time of the driving circuit divided by two: $T_D > t_r/2$.

The circuit of Figure 7-2 can be redrawn as shown in Figure 7-3 to include the equivalent circuit of the MECL gate. The resistor, R_O, is the output source



7-2: MECL Gate Driving a Transmission Line

7-3: Equivalent MECL Gate Output, Driving a Transmission Line



impedance (for MECL 10,000 it is 7 ohms, and MECL III it is 5 ohms). According to theory, the rise time of the driving voltage source is not affected by the capacitance of the transmission line. Except for skin effect and dielectric losses, the signal will remain undistorted until it reaches the load. The equation representing the voltage waveform going down the line as a function of distance and time can be written as:

$$V_1(X, t) = V_A(t) \bullet U(t - Xt_{pd}), \text{ for } t < T_D \ , \tag{1}$$

where:

$$V_A(t) = E_S(t)\left(\frac{Z_o}{Z_o + R_o}\right),$$

V_A = voltage at point A,
X = the distance to an arbitrary point on the line,
ℓ = total line length,
t_{pd} = propagation delay of the line in ns/unit distance,
$T_D = \ell\, t_{pd}$,
$U(t)$ = a unit step function occurring at $t = 0$, and
$E_S(t)$ = the source voltage at the sending end of the line.

When the incident voltage V_1 reaches the end of the long line, a reflected voltage, V'_1, will occur if $R_L \neq Z_o$. The reflection coefficient at the load, ρ_L, can be obtained by applying Ohm's Law.

The voltage at the load is $V_1 + V'_1$ which must be equal to $(I_1 + I'_1)\, R_L$. But $I_1 = V_1/Z_o$, and $I'_1 = -V'_1/Z_o$ (the minus sign is due to V'_1 travelling toward the source). Therefore,

$$V_1 + V'_1 = \left(\frac{V_1}{Z_o} - \frac{V'_1}{Z_o}\right) R_L \ . \tag{2}$$

By definition,

$$\rho_L = \frac{\text{reflected voltage}}{\text{incident voltage}} = \frac{V'_1}{V_1} \ .$$

Solving for V'_1/V_1 in equation 2, and substituting in the relation for ρ_L results in:

$$\rho_L = \frac{R_L - Z_o}{R_L + Z_o} \ . \tag{3}$$

Similarly, the reflection coefficient at the source is:

$$\rho_S = \frac{R_o - Z_o}{R_o + Z_o} \ . \tag{4}$$

By summing the incident voltage, V_1 (eq. 1), together with similar voltage contributions from the various orders of reflection (due to ρ_L and ρ_S), a general equation for total line voltage can be written, and used to develop practical design information:

$$V(X,t) = V_A(t)\Big[U\left(t - t_{pd}X\right) + \rho_L U\left(t - t_{pd}(2\ell - X)\right)$$

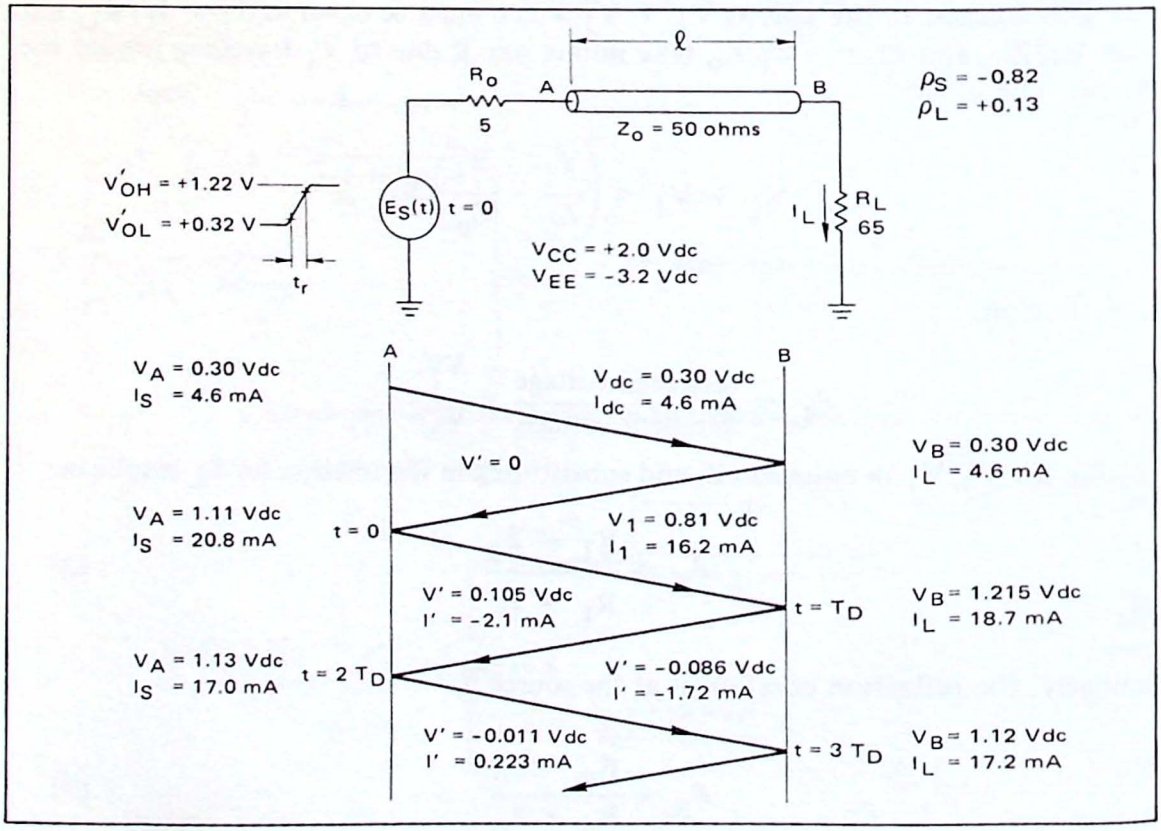
$$+ \rho_L\rho_S U\left(t - t_{pd}(2\ell + X)\right) + \rho_L{}^2\rho_S U\left(t - t_{pd}(4\ell - X)\right)$$

$$+ \rho_L{}^2\rho_S{}^2 U\left(t - t_{pd}(4\ell + X)\right) + \ldots\Big] + V_{dc} \qquad (5)$$

Note that as time progresses, the U step function brings successively higher order reflection coefficient terms into V (X, t). Successive terms may be positive or negative, depending on the resulting sign, and so damped ringing can occur. Equation 5 expresses the voltage at any point on the line, X, for any time, t. The equation can be used graphically with a lattice diagram (as explained in References 5 and 6), to find V (X, t).

Example 1. Figure 7-4 will be used to illustrate the lattice diagram method for

7-4: Lattice Diagram for a Typical Reflection Example



finding V (X, t) and the use of equation 5. The source impedance of the MECL III gate is 5 ohms, resulting in a reflection coefficient at the source of -0.82 for a line impedance of 50 ohms.

The load resistor is arbitrarily chosen to be 30 percent greater (65 ohms) than the characteristic impedance (50 ohms) so that reflections will occur. The resulting reflection coefficient at the load is $\rho_L = +0.13$. Two vertical lines are drawn to represent the input of the line, point A, and the output of the line, point B. A line is drawn from point A to point B before t = 0 to represent the steady state conditions. Note that for $V_{CC} = +2$ V and $V_{EE} = -3.2$ volts, the nominal logic levels are approximately logic $\emptyset = 0.3$ volts, and logic 1 = 1.14 volts. (These power supply conditions are used to permit convenient measurements when output resistors are returned directly to ground). For steady state conditions, the line looks like a short line with a resistance equal to R_{dc}. It can be assumed that R_{dc} is negligible for this example.

The voltage and current at points A and B are the same initially, as shown in the diagram. At t = 0, the voltage at the source switches from a logic $\emptyset$ to a logic 1 level. The voltage term, $V_A(t)$, in equation 1 is:

$$V_A(t) = (V'_{OH} - V'_{OL}) \left(\frac{Z_o}{Z_o + R_o} \right) = V_1 = 0.81 \text{ volt},$$

where:

$$(V'_{OH} - V'_{OL}) = E_S(t) = \text{internal voltage swing in the circuit.}$$
$$= \Delta V_{INT}$$

Therefore, at time t = 0 a voltage waveform, $V_1 = 0.81$ volt, and a current, $I_1 = 16.2$ mA, travel down the line – as shown in the diagram by the line from t = 0 to $t = T_D$ (T_D is the time it takes for the wavefront to travel down the length of line, ℓ). Next, a line is drawn from $t = T_D$ to $t = 2T_D$. Voltage and current values are indicated. Note that here the reflected current is negative, indicating the current is flowing back toward the source; the reflection coefficient for the current is a minus one times the reflection coefficient for the voltage.

To find the voltage at point B for $t = T_D$ all the voltages arriving at and leaving from this point are summed. The same is done to determine the load current. The process continues until the voltage at the load approaches the new steady state condition – in the example, when $t = 3T_D$. (The steady state logic 1 voltage is actually 1.13 volts).

This example indicates that for a case in which the load resistor is 30% higher than the characteristic impedance, 85 mV of overshoot and 10 mV of undershoot would occur. Generally, as far as noise immunity is concerned, only the undershoot need be considered. The typical noise immunity (or noise margin) for a MECL circuit is greater than 200 mV. Since the undershoot in this example was 10 mV, the typical noise immunity would exceed 190 mV. In actual system design, typically more than 100 mV of undershoot can be tolerated. Regarding overshoot, 300 mV can be tolerated, except in some early ac coupled flip-flops (MECL I and II). This restriction insures that saturation of the input transistor does not occur (if it did, the gate would slow down). If a 100 ohm load resistor were used in Figure 7-4, the resulting overshoot would be about 220 mV and the undershoot, about 80 mV. In effect then, if the load resistor is twice the characteristic impedance, the noise margin is typically 120 mV – which is more than acceptable for MECL circuits.

A slightly different situation can exist when the output of the MECL gate switches from a logic 1 to a logic ∅. The output of the MECL gate will turn off if the termination resistor, R_L, is somewhat larger than the characteristic impedance of the line. For the conditions in Figure 7-4, the output transistor of the MECL gate will turn off at t = 0 for the negative going transition, when $R_L > 70$ ohms.

An equation for the value of R_L at which the gate will turn off can be derived as follows. The maximum voltage change at point A, Figure 7-4, (due to turning off the output transistor) is the product of the dc current in the line and the characteristic impedance of the line:

$$\Delta V_A = I_{LINE}(Z_o) = \frac{V'_{OH}}{R_o + R_L}(Z_o) .$$

The voltage at point A is also dependent on the internal resistance of the driving gate R_o and the internal logic swing:

$$\Delta V_A = \frac{Z_o}{R_o + Z_o}(\Delta V_{INT}) .$$

Equating the two and solving for R_L:

$$R_L = \frac{V'_{OH}(R_o + Z_o)}{\Delta V_{INT}} - R_O . \qquad (6)$$

Thus for the conditions given in Figure 7-4, the output transistor will turn off at t = 0 when $R_L = \frac{1.22(5 + 50)}{0.9} - 5 = 70\Omega$ is exceeded.

The case for which the MECL output turns off is not in itself a serious problem, although it makes a thorough analysis more difficult. Two reflection coefficients must be used at the sending end, and a piecewise approach used in determining the voltage reflections.

Example 2. The condition for a negative-going transition will now be analyzed (cf Figure 7-5.) The steady state high logic level current is:

$$I_{dc} = \frac{V'_{OH}}{R_o + R_L} = 11.6 \text{ mA} .$$

For the conditions shown in Figure 7-5, the use of equation 6 shows that the load resistor is indeed larger than required to turn off the output transistor during a negative transition.

To determine the voltage V_1 at t = 0, the following equation results from the application of Ohm's Law to the circuit:

$$V_1 = -\left(I_{dc} + \frac{V_A + 3.2 + V_1}{R_E}\right) Z_o . \qquad (7)$$

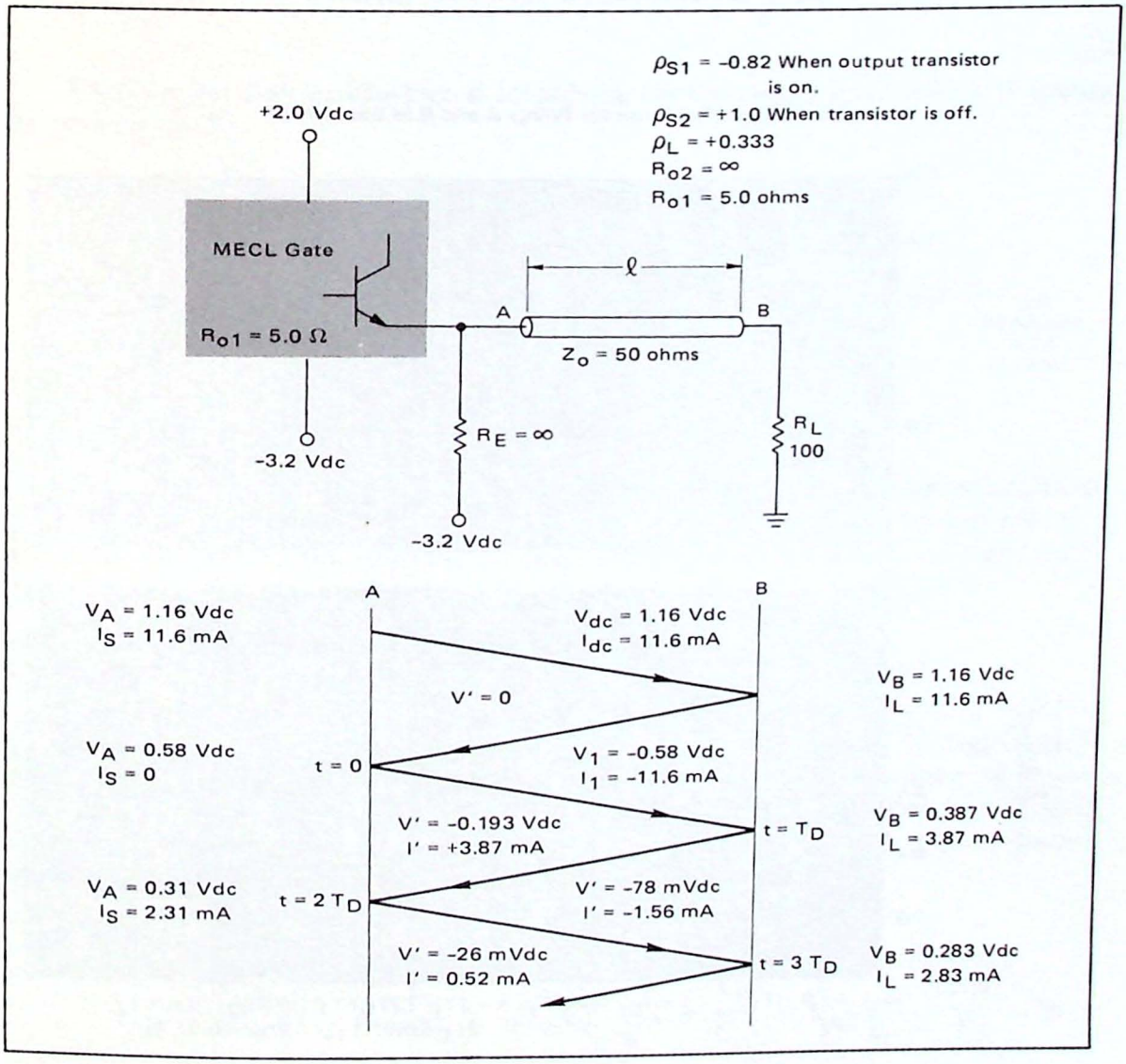
For the example shown, let $R_E = \infty$, then:

$$V_1 = -I_{dc}Z_o \cdot \tag{8}$$

Solving equation 8, $V_1 = -0.58$ volt. The implication of this result is that stubbing off the line with gate loads in a distributed fashion is not recommended, due to the reduced intital voltage swing. However, it would be acceptable to lump the loads at the end of the line (as will be shown).

Since the value of the load resistor is greater than the characteristic impedance, the voltage swing at the load resistor is greater than V_1 by the amount of $\rho_L V_1$ (in this example, 193 mV). When $t = T_D + T_1$, the voltage at B is equal to 0.387 volt; so 82 mV of undershoot occurs. Undershoot on the falling edge is defined as the amount of voltage step above the nominal logic ∅ level of 0.305 volt. Overshoot in the low logic state is defined as the amount of voltage change below the logic ∅ level.

7-5: Lattice Diagram for Negative-Going Voltage Transition



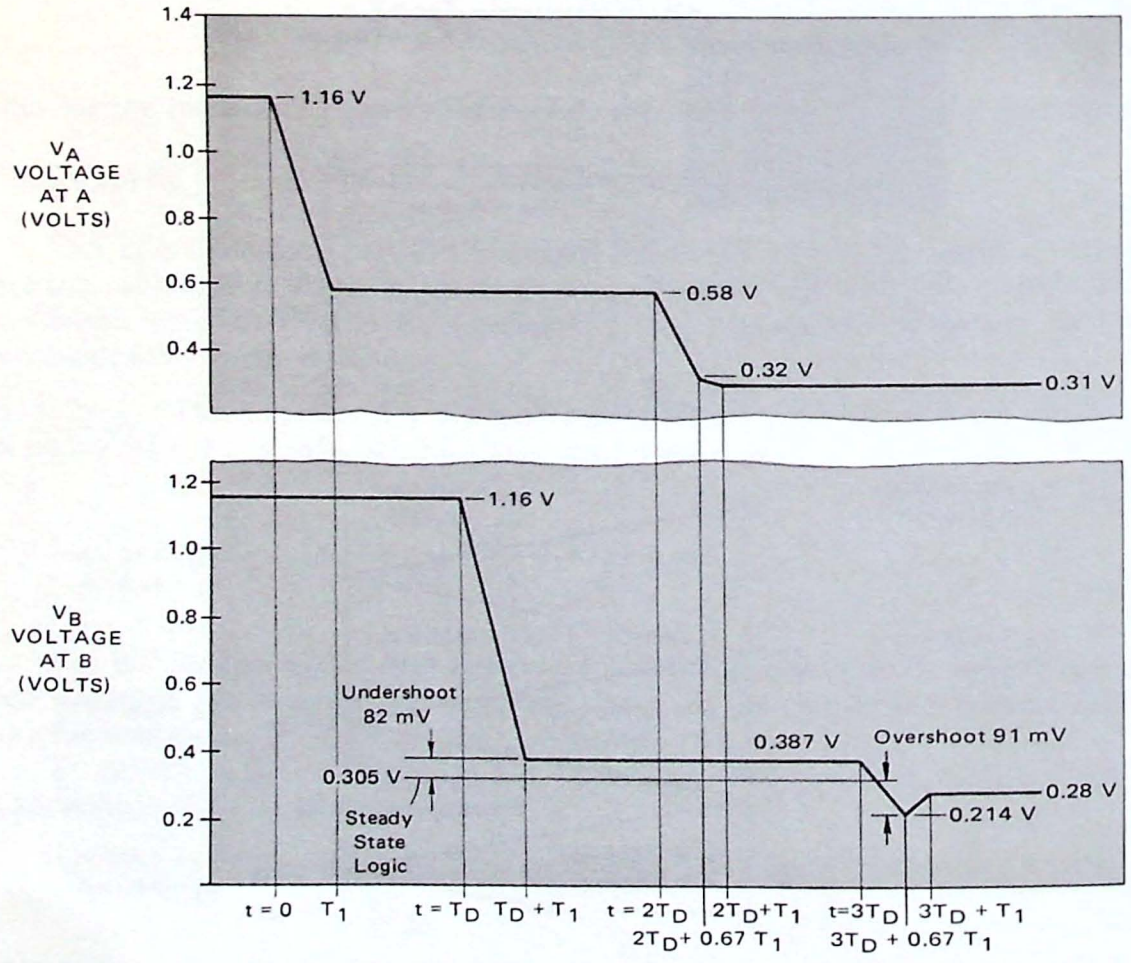
In Figure 7-6, the voltage waveforms at points A and B of this example are shown as a function of time. To be more realistic, the waveform in the figure is shown to be a negative-going ramp rather than an abrupt step function. The term, T_1, is the amount of time it takes for the waveform at A to switch to the level at which the output transistor turns off. The fall time of the signal would have been longer by an amount equal to $T_1' = \frac{(1.16 - 0.305)}{(1.16 - 0.58)} T_1$, if the termination resistor had been 70 ohms or less.

The reflected voltage waveform leaving point B at $t = T_D$ arrives at point A at $t = 2T_D$. The source impedance is very high initially ($\rho_S = +1.0$), with the output transistor being in the off condition until the voltage at A falls to 0.32 volt. Then, the source impedance changes to 5 ohms ($\rho_S = -0.82$). The following formula may be used to determine the point at which the transistor turns on:

$$\Delta V_{source} = V_1 + \rho_S V_1 = 2V_1 \quad \text{(valid prior to transistor conduction),} \tag{9}$$

where V_1 is now the incident voltage approaching the source and ΔV_{source} is the change in voltage at the source necessary to turn the transistor on.

7-6: Voltage Waveforms for Points A and B in Example 2



In this example the actual voltage change for conduction to occur is: $\Delta V_{source} = 0.32 - 0.58 = -0.26$ volt. Therefore, the voltage waveform approaching the source (193 mV) can be broken into two signals, $V_{11} = -0.13$, and $V_{12} = -0.063$ volt. The reflected voltage due to V_{11} is $V'_{11} = -0.13$ volt, and for V_{12}, the reflected voltage is $V'_{12} = (-0.82)(-0.063) = +0.052$ volt. The two reflected voltages of opposite polarity at point A going toward point B are the reason for the increased overshoot of short duration at point B, when $t = 3T_D + \left(\frac{0.13}{0.193}\right) T_1$ (see Figure 7-6).

The steady state voltage reflection that occurs after $t = 2T_D + T_1$ is the sum of -0.13 volt and +0.052 volt, equal to -78 mV as shown in Figure 7-5. The steady state voltage reflection can be calculated using the relation:

$$V' = \rho_{S2}\Delta V_{source}\left(\frac{1 + \frac{Z_o}{R_{o2}}}{2}\right) + \rho_{S1}\left[V_1 - \Delta V_{source}\left(\frac{1 + \frac{Z_o}{R_{o2}}}{2}\right)\right]. \quad (10)$$

Equation 10 may be illustrated by solving for the steady state reflection voltage at $t = 2T_D + T_1$:

$$V' = (+1.0)(0.32 - 0.58)\left(\frac{1 + \frac{50}{\infty}}{2}\right) + (-0.82)\left[-0.193 - (0.32 - 0.58)\left(\frac{1 + \frac{50}{\infty}}{2}\right)\right] = 78 \text{ mV}.$$

From the analysis of Figure 7-5, it is concluded that the MECL gate can safely drive the transmission line ($Z_o = 50$ ohms) with a 100 Ω load resistor and with the gate loads lumped at the end of the line, since less than 100 mV of undershoot occurs. The remaining noise margin will be typically greater than 100 mV.

Signal Propagation Delay for Microstrip and Strip Lines with Distributed or Lumped Loads

The propagation delay, t_{pd}, has been shown in Chapter 3 to be 1.77 ns/ft for microstrip lines and 2.26 ns/ft for strip lines, when a glass epoxy dielectric is the surrounding medium. The propagation delay time of the line will increase with gate loading and the altered delay can be derived as follows. The unloaded propagation delay for a transmission line is $t_{pd} = \sqrt{L_o C_o}$. If a lumped load, C_d, is placed along the line, then the propagation delay will be modified to t'_{pd}:

$$t'_{pd} = \sqrt{L_o(C_o + C_d)} = \sqrt{L_o C_o}\sqrt{1 + \frac{C_d}{C_o}} = t_{pd}\sqrt{1 + \frac{C_d}{C_o}}, \quad (11)$$

where L_o and C_o are the intrinsic line inductance and capacitance per unit length.

Therefore, the signal propagation down the line will increase by the factor of:

$$\sqrt{1 + \frac{C_d}{C_o}} .$$

A MECL gate input should be considered to have 5 pF of capacitance for ac loading considerations (includes stray capacitance). If 4 gate loads are placed on a 1 foot signal line, then the distributed capacitance, C_d, is equal to 20 pF/ft or 1.67 pF/in. As an example, assume that it is desired to find the propagation delay increase for a 50-ohm microstrip line on a glass epoxy board. From Figure 3-7 assume that the line width is chosen to be 25 mils; then the dielectric material should have a thickness of 15 mils to yield $Z_o = 50\Omega$. From Figure 3-8, the capacitance of the line is 35 pF/ft. Therefore, the modified propagation delay would be:

$$t'_{pd} = 1.77 \text{ ns/ft} \sqrt{1 + \frac{20}{35}} = 2.21 \text{ ns/ft} .$$

For a 50-ohm strip line on a glass epoxy board with a 15 mil spacing between the strip line and ground plane, a 12 mil width would be required (cf Figure 3-9). From Figure 3-10, the strip line would exhibit a capacitance of 41 pF/ft.

The modified propagation delay for such a strip line would be:

$$t'_{pd} = 2.26 \text{ ns/ft} \sqrt{1 + \frac{20}{41}} = 2.75 \text{ ns/ft} .$$

Notice that the propagation delay for the strip line and the microstrip line change by approximately the same factor when the separation between the line and ground plane, and the characteristic impedance are the same. However the line width of the strip line is less (by a factor of 2) than the microstrip line for the same characteristic impedance.

It should be noted that to obtain the minimum change and lowest propagation delay as a function of gate loading, the *lowest* characteristic impedance line should be used. This will result in the largest intrinsic line capacitance. With MECL 10,000 the lowest impedance that can be used is about 35 ohms ($V_{TT} = -2.0$ volts, $R_{TT} = 35$ ohms).

According to theory (Reference 1), whenever an open line (stub) is driven by a pulse, the resultant undershoot and ring are held to about 15 percent of the logic swing if the two way delay of the line is less than the rise time of the pulse. The maximum line length, ℓ_{max}, may be calculated using the equality:

$$\ell_{max} = \frac{t_r}{2t'_{pd}} \text{ (inches)} ,$$

where t_r is the rise time of the pulse in nanoseconds, and t'_{pd} is the modified propagation delay in nanoseconds/inch from equation 11.

A quadratic equation for maximum line length for G-10 fiber glass epoxy microstrip conductors may be written in terms of C_D C_o and t_r as:

$$\ell^2_{max} + \frac{C_D}{C_o}\ell_{max} - 11.1\ t_r^2 = 0\text{, (for microstrip lines),} \quad (12)$$

where C_D is total gate capacitance.

An equation for maximum open line length for a strip line (using G-10 fiber glass epoxy material) can be written in a similar fashion. The result is:

$$\ell^2_{max} + \frac{C_D}{C_o}\ell_{max} - 7.1\ t_r^2 = 0, \quad \text{(for strip lines).} \quad (13)$$

Using the lattice diagram, it has been found that the rule of thumb used to derive equations 12 and 13 should be modified for an open line because the incident voltage doubles at the end of the line. This results in a faster rise time at the receiving end of an unloaded line than at the driving end. An approximate value of maximum open line length can be generated from equations 12 and 13 if the rise time that is substituted into the equations is multiplied by an adjustment factor, 0.75. This maintains an approximate overshoot and undershoot of less than 35% and 12% respectively.

To demonstrate how equations 12 and 13 may be used, the maximum open line length will be computed for a 50 ohm line with a fanout of one MECL 10,000 gate. Using the equation $t_{pd} = Z_o C_o$, the line capacitance, C_o, is found to be $C_o = 2.96$ pF/in for microstrip, and $C_o = 3.76$ pF/in for strip line. For a fanout of one, C_D is equal to 5 pF when the device is in a socket. The rise time for MECL 10,000 is 3.5 ns which means that a value of $t_r = 0.75 \times 3.5 = 2.6$ ns should be used in the equations. Solving equations 12 and 13, $\ell_{max} = 7.9$ inches for a 50 ohm microstrip line and $\ell_{max} = 6.2$ inches for a 50 ohm strip line.

Equations 12 and 13 can be very useful in finding the approximate maximum line length under various conditions. However if overshoot or undershoot differing from the above values is specified, equations 95 and 103 (derived later in this chapter) should be used for defining maximum line length. The exact voltage at the end of an open line with loading is also derived later in this chapter, and leads to equation 87. Using that equation, a computer program has been written in which the maximum line length is calculated when maximum overshoot and undershoot are specified. Figures 3-13, 3-14, and 3-15 show the results of the program. Note that the tables give the maximum line lengths for fanouts of 1, 2, 4, and 8 for various types of lines with a wide range of characteristic impedances.

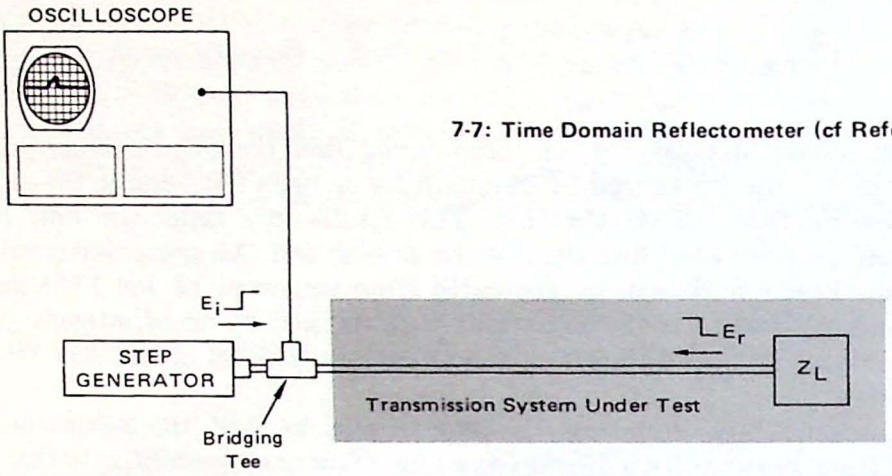
The maximum line lengths are also given for various characteristic impedances in the backplane. The characteristic impedance of the backplane should be between 100 and 180 ohms if a ground screen is used. For MECL 10,000 from Table 3-13, 5.9 inches of open backplane wiring can be driven for a fanout of one.

It should be remembered that these line lengths are based on 100 mV maximum undershoot, and are not absolute maximum lengths with which MECL circuits will operate. It is possible to use longer unterminated lines than shown – the tradeoff being an associated loss of noise immunity due to increased ringing.

From these calculations, it can be concluded that lower impedance lines result in longer line lengths before termination is required. The lower impedance lines are preferred over higher impedance lines because longer open lines are possible, and the propagation delay down the line is reduced. In addition, more stubbed-off gate loads can be driven with a terminated line due to its higher capacitance per unit length.

Microstrip Transmission Line Techniques, Evaluated Using TDR Measurements

The time domain reflectometer (TDR) employs a step generator and an oscilloscope in a system which might be described as "closed-loop radar" (cf Figure 7-7). In operation, a voltage step is propagated down the transmission line under investigation. Both the incident and reflected voltage waves are monitored on the oscilloscope at a particular point on the line.



7-7: Time Domain Reflectometer (cf Reference 7)

The incident voltage step, E_i, is a positive edge with an amplitude of 1 volt and a rise time of 30 ps. It is generated by a tunnel diode, which has a source impedance of 50 ohms (HP 1817A sampler, or equivalent). Also, the output edge has very little overshoot (less than ±5%).

This TDR technique reveals the characteristic impedance of the line under test. It shows both the position and the nature (resistive, inductive, or capacitive) of each discontinuity along the line, and signifies whether losses in a transmission system are series losses or shunt losses. All of this information is immediately available from the oscilloscope's display (cf Reference 7). An example of a microstrip line evaluated with TDR techniques is shown below.

TDR Example 1.

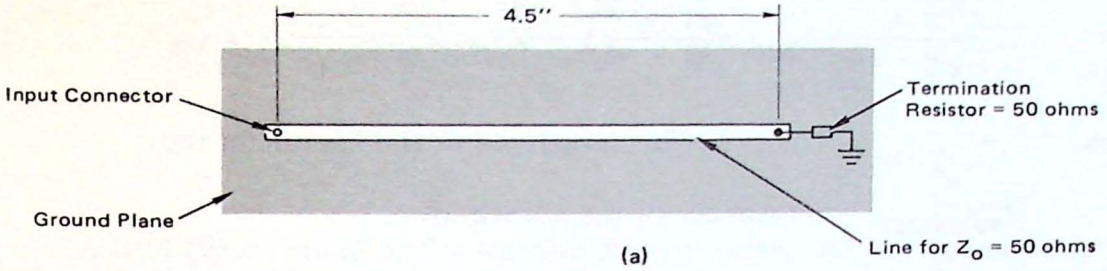
Board material:	Norplex Type G-10;
Dielectric thickness:	$h = 0.062$ inch;
Copper thickness:	$t = 0.0014$ inch;
Dielectric constant:	$e_r = 5.3$.

The formula for the characteristic impedance given in Chapter 3 was:

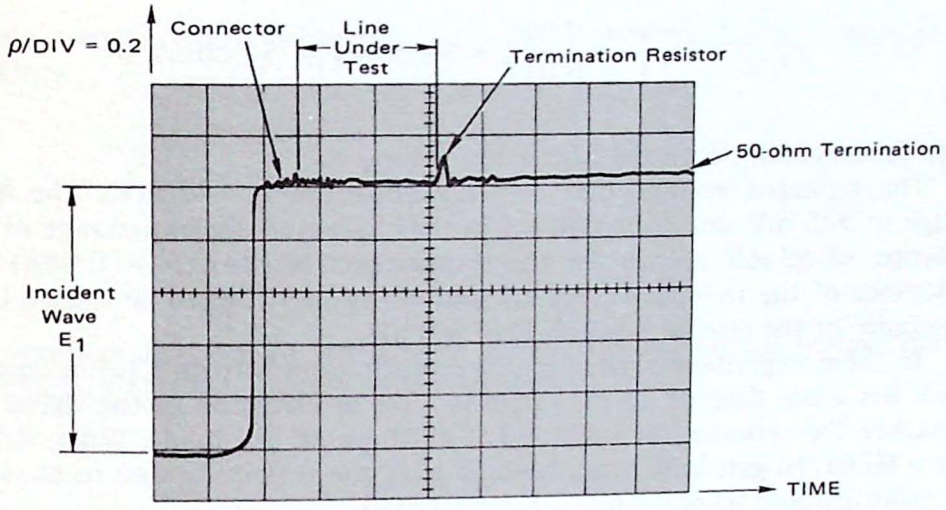
$$Z_o = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98\,h}{0.8\,w + t}\right). \qquad (14)$$

For a line width, $w = 0.1$ inch, the characteristic impedance of the line is calculated to be 51 ohms. A board was fabricated as shown in Figure 7-8(a) to the dimensions specified above. Figures 7-8(b) and 7-8(c) show the incident and reflected

7-8: TDR Determination of Line Characteristic Impedance

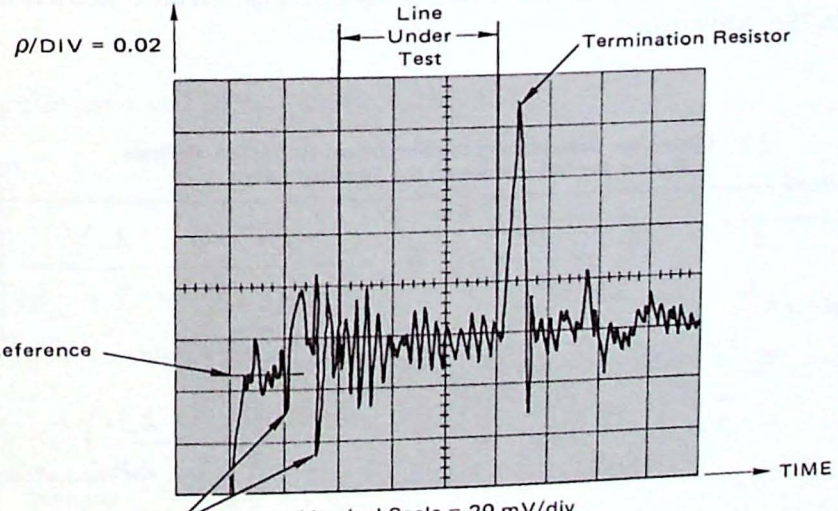


(a)



(b)

Vertical Scale = 200 mV/div
Horizontal Scale = 0.6 ns/div



(c)

Vertical Scale = 20 mV/div
Horizontal Scale = 0.4 ns/div

waveforms observed with the TDR. The vertical scale is calibrated both in terms of the voltage and the reflection coefficient, ρ. Equation 3 can be rearranged to determine the characteristic impedance of the line:

$$Z_{line} = \left(\frac{1 + \rho}{1 - \rho}\right) \cdot Z_{reference} \quad , \tag{15}$$

where: Z_{line} = characteristic impedance of the line under test,

$Z_{reference}$ = impedance of the known line.

The 50 ohm reference point is shown in Figure 7-8(c). The mean level of the reflected waveform due to the line has a $\rho = +0.01$. Substituting values into equation 15 permits calculation of the line impedance:

$$Z_{line} = \left(\frac{1 + 0.01}{1 - 0.01}\right) \cdot 50 \text{ ohms} = 51 \text{ ohms} \quad ,$$

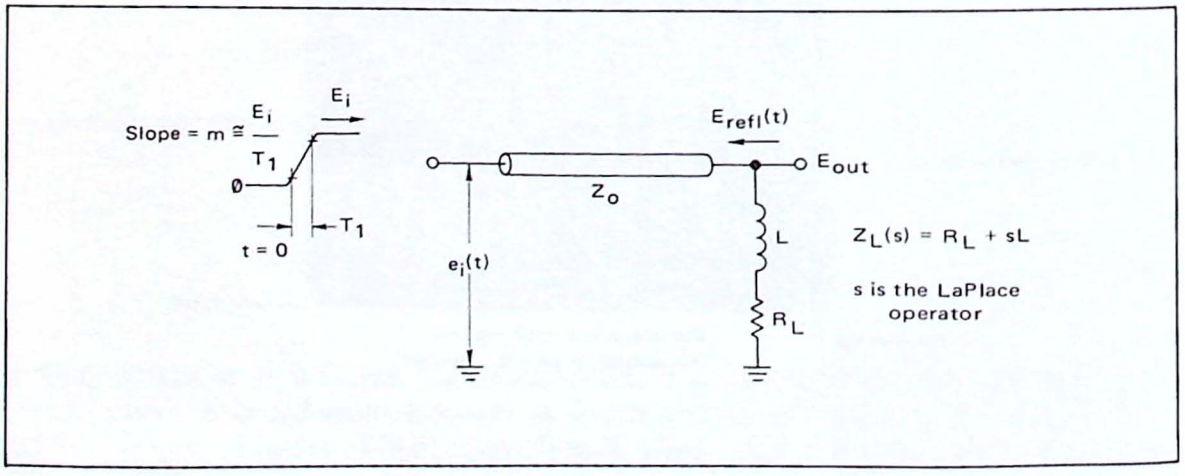
which agrees closely with the calculated value.

The reflected voltage due to the connector is ±40 mV. The line reflects a voltage of ±25 mV due to variations in the characteristic impedance of the line. The reflection of 88 mV shown for the termination resistor ($\rho = 0.088$) is due to the inductance of the resistor. It was calculated (by methods to be shown later) that the inductance of the resistor was less than 0.9 nH.

In these experiments, the input waveform comes from a tunnel diode generator which has a rise time of 28 ps. There is some attenuation of the signal noticeable as it reaches the termination resistor (t_r = 80 ps at the load). When driving the line with a MECL III gate with a rise time of 1 ns, the reflection due to the inductance of the resistor would be much less (about 10 mV).

TDR Example 2: An equation can be derived to determine the maximum reflection voltage due to the inductance of the resistor leads. The circuit shown in Figure 7-9 will be used in the derivation.

7-9: Circuit for Determining the Maximum Reflected Voltage Due to the Inductance of the Resistor Leads



The reflection coefficient at the load is:

$$\rho_L(s) = \frac{Z_L - Z_o}{Z_L + Z_o} = \frac{(R_L + sL) - Z_o}{(R_L + sL) + Z_o} = \frac{s + \dfrac{R_L - Z_o}{L}}{s + \dfrac{R_L + Z_o}{L}}, \qquad (16)$$

where s is the LaPlace operator for $j\omega$. The driving voltage will be represented as:

$$e_i(t) = mt\,U(t) - m(t - T_1)\,U(t - T_1), \qquad (17)$$

where U(t) is a step function occurring at t = 0. Taking the LaPlace transform of equation 17 gives:

$$E_i(s) = \frac{m}{s^2}\left(1 - e^{-T_1 s}\right). \qquad (18)$$

The reflected voltage at the load is then the product of the driving voltage and the reflection coefficient (both in the transformed plane):

$$E_{refl}(s) = E_i(s)\rho_L(s) = \frac{s + \dfrac{R_L - Z_o}{L}}{s^2\left(s + \dfrac{R_L + Z_o}{L}\right)} \cdot m\left(1 - e^{-T_1 s}\right). \qquad (19)$$

Taking the inverse LaPlace transform yields:

$$E_{refl}(t) = \left[\frac{2Z_oL}{(R_L + Z_o)^2} + \left(\frac{R_L - Z_o}{R_L + Z_o}\right)t - \left(\frac{2Z_oL}{(R_L + Z_o)^2}\right)e^{-\frac{(R_L + Z_o)t}{L}}\right] mU(t) -$$

$$\left[\frac{2Z_oL}{(R_L + Z_o)^2} + \left(\frac{R_L - Z_o}{R_L + Z_o}\right)(t - T_1) - \left(\frac{2Z_oL}{(R_L + Z_o)^2}\right)e^{-\frac{(R_L + Z_o)(t - T_1)}{L}}\right]$$

$$mU(t - T_1). \qquad (20)$$

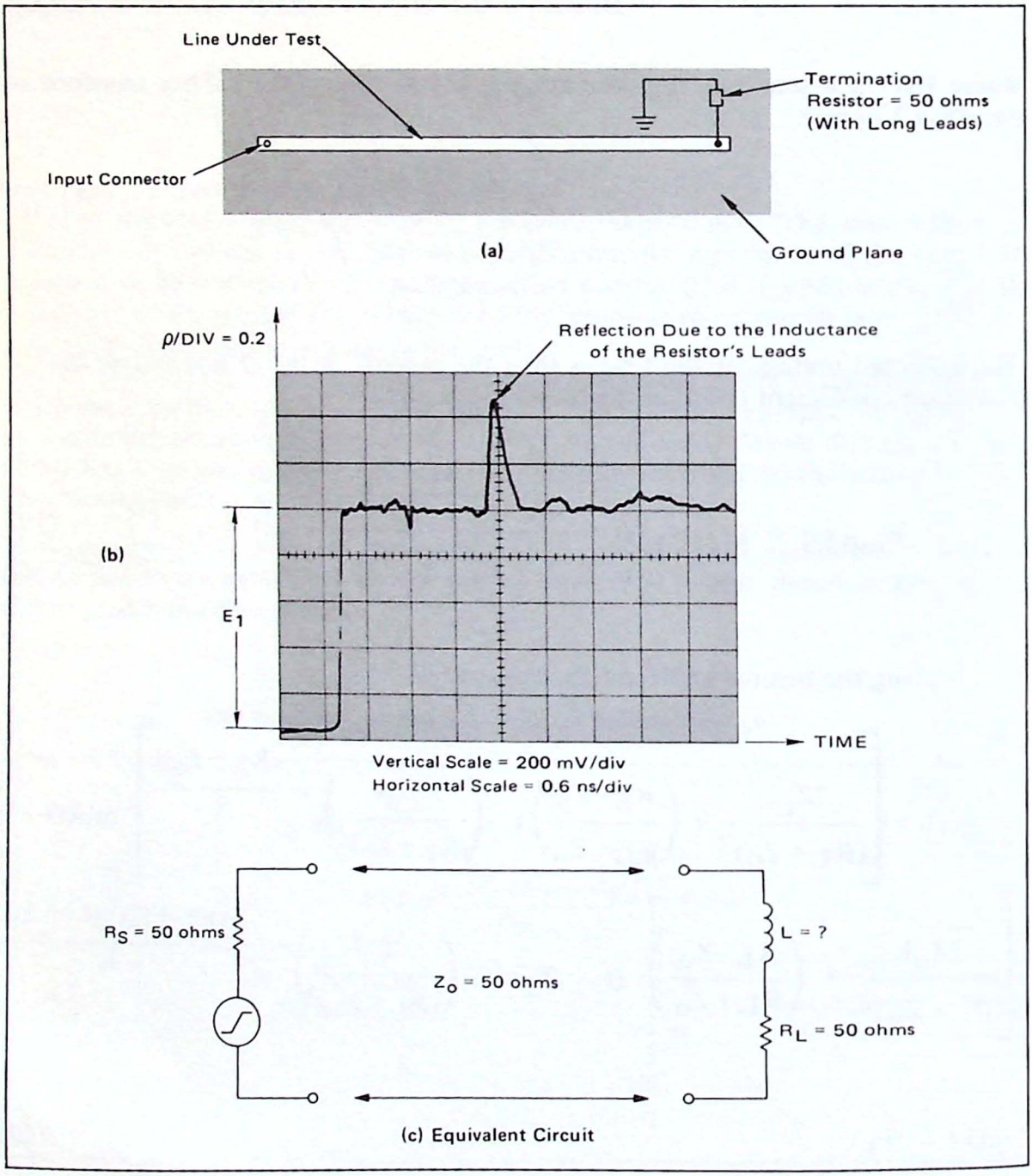
The maximum reflection voltage occurs at $t = T_1$. Then, for $R = Z_o$:

$$E_{refl}(t = T_1) = E_{refl\,max} = \frac{mL}{2Z_o}\left(1 - e^{-\frac{2Z_o}{L}T_1}\right). \qquad (21)$$

This equation relates the maximum reflected voltage, which can be measured by TDR, and the inductance, which can then be calculated for the circuit of Figure 7-9.

TDR Example 3. This example indicates how to measure the effect of resistor leads using the TDR. Figure 7-10(a) shows the construction of a microstrip board used for

7-10: Effects Due to Termination Resistor Leads



determining the effects of a resistor with 1" lead lengths. The reflected voltage determined from the TDR measurement is 480 mV (see Figure 7-10(b)). The rise time at the input to the line is 28 ps but it is lengthened to about 80 ps as the wavefront reaches the termination resistor.

The time, T_1, associated with the slope of the input voltage rise at the terminating resistor can be approximated as:

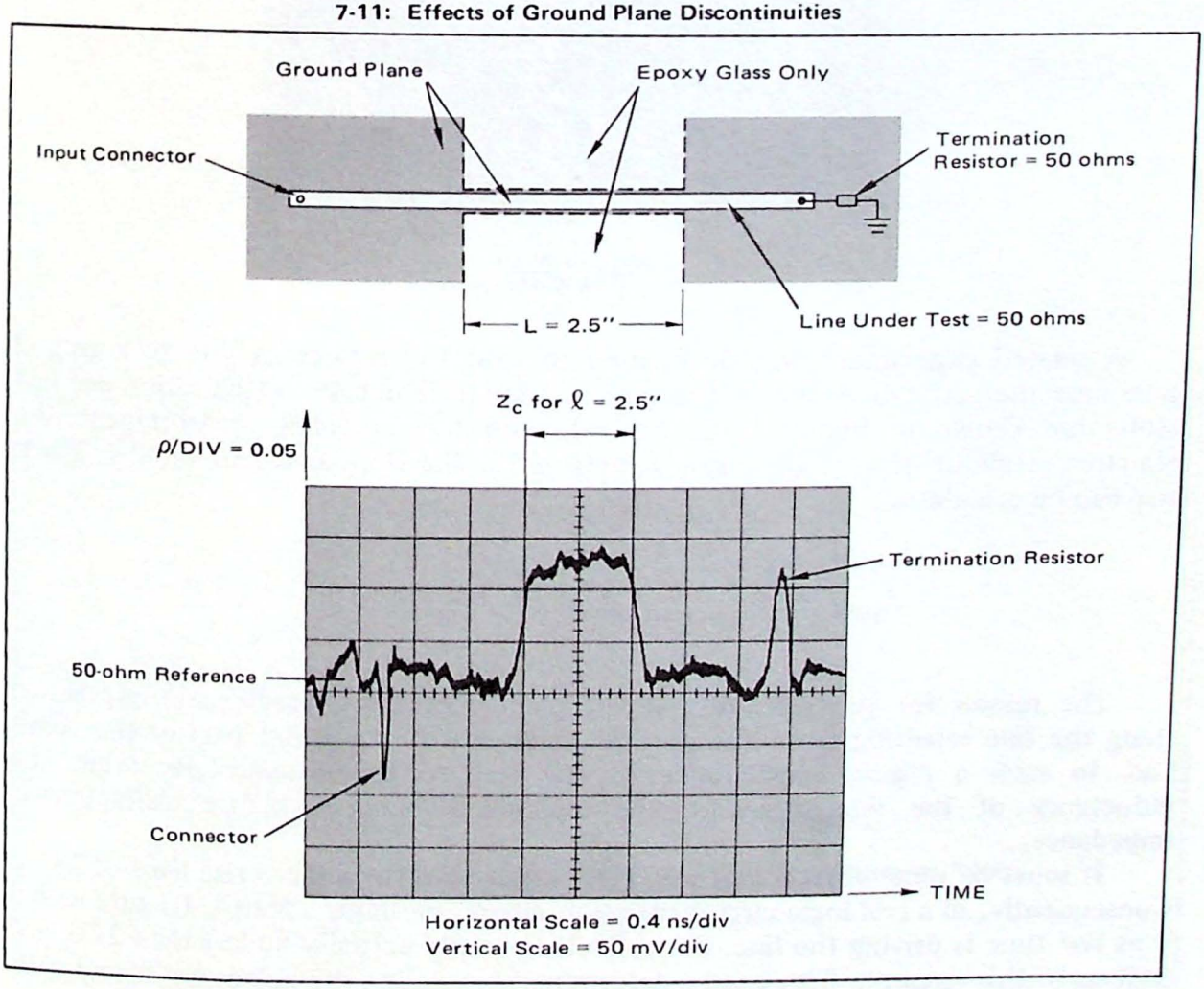
$$T_1 \approx \frac{t_r}{0.80} = 100 \text{ ps.} \qquad (22)$$

The inductance can be computed by using equation 21, giving L = 6 nH. Additional information can be obtained from the decay of the reflection shown in Figure 7-10(b). The decay lasts about 0.3 ns, implying a time constant of about 0.3 ns/5 = 60 ps (using 5 time constants as a decay time). The calculated time constant for an inductance of 6 nH is: $L/2Z_o$ = 60 ps. The two results agree closely.

When driving the line with a MECL III gate – rise time = 1 ns – the reflection would be only 50 mV. Most carbon resistor types will have less than 10 nH of inductance. This inductance gives a reflection < 75 mV when the line is driven by a MECL III gate. Note that the reflection is positive, indicating that the noise immunity of a MECL gate connected at the load would be unchanged.

TDR Example 4. Experiments have also been performed to determine the effects of a ground plane on the characteristic impedance of microstrip lines. Figure 7-11

7-11: Effects of Ground Plane Discontinuities



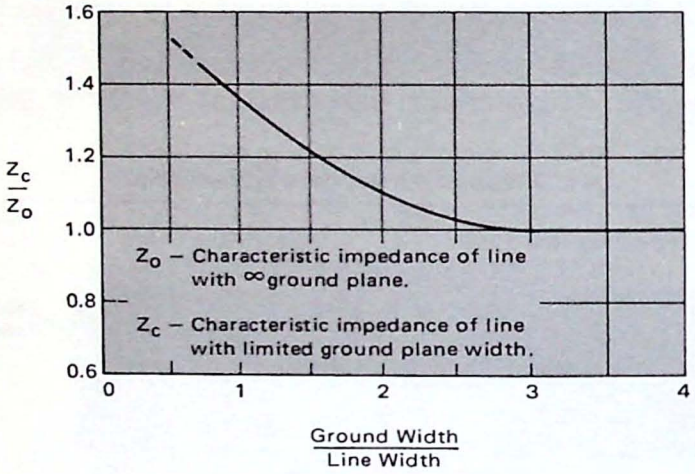
illustrates what happens when the ground plane width under the transmission line abruptly drops to the width of an active line. The TDR waveform shows that a 12% reflection occurs due to this discontinuity in the ground plane.

Using equation 15 the impedance of the 2-1/2 inch-long strip can be calculated as:

$$Z_{line} = \frac{1 + 0.12}{1 - 0.12} \cdot 50 = 68 \text{ ohms.}$$

Figure 7-12 shows a curve that approximates the change in the characteristic impedance of the line for various ratios of ground plane width to active line width. Note that when the ground width is greater than 3 times the line width, the characteristic impedance is constant according to equation 14.

7-12: Variation of Microstrip Impedance as a Function of Ground Width ÷ Line Width



A related experiment was performed to find the reflection due to a ground plane near the active line, but not directly under it. The test configuration and test results are shown in Figure 7-13. As indicated by the TDR measurement, the reflection is about 36%. Again using equation 15, the impedance of the 2-1/2 inch strip can be calculated:

$$Z_{line} = \frac{1 + 0.36}{1 - 0.36} \cdot 50 = 106 \text{ ohms.}$$

The reason for the reflection is the change in the characteristic impedance along the line resulting from the ground plane not being under part of the active line. In such a region, capacitance of the line to ground *decreases* while the inductance of the line *increases*, the net result being a higher characteristic impedance.

It must be remembered that the TDR input waveform has a rise time of 28 ps. Consequently, in a real logic circuit situation where, perhaps, a MECL III gate with a 1 ns rise time is driving the line, the reflection would actually be less than 27%, not 36% as in this example. This can be determined by scaling the value of ρ found with

the TDR waveshape in Figure 7-13(b), with a 1 ns rise time. When the length of the ground plane discontinuity is less than the distance travelled by the signal during its rise time, then the reflection coefficient can also be calculated as:

$$\rho' = \frac{2\ell\, t_{pd}}{t_r} \cdot \rho, \quad \text{for } \frac{2\ell\, t_{pd}}{t_r} < 1 \quad , \tag{23}$$

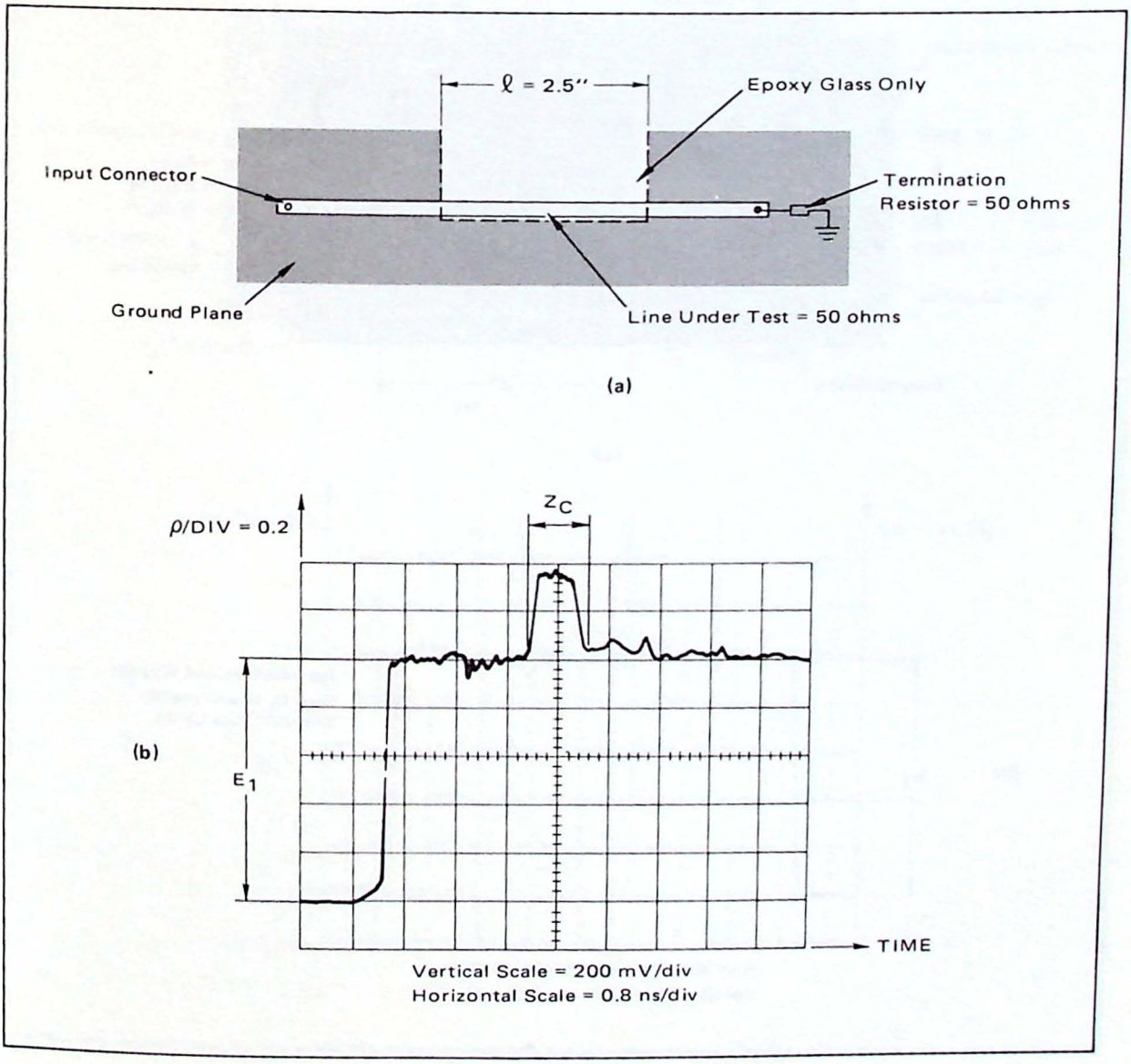
where: t_{pd} = the propagation delay time of the line in ns/in.

t_r = the rise time of the signal in ns,

ℓ = the length of the discontinuity in inches,

ρ = the reflection coefficient for $2\ell t_{pd}/t_r \geq 1$ (in this case the value found with the TDR waveshape with t_r = 28 ns).

7-13: Effects of Ground Plane Discontinuity



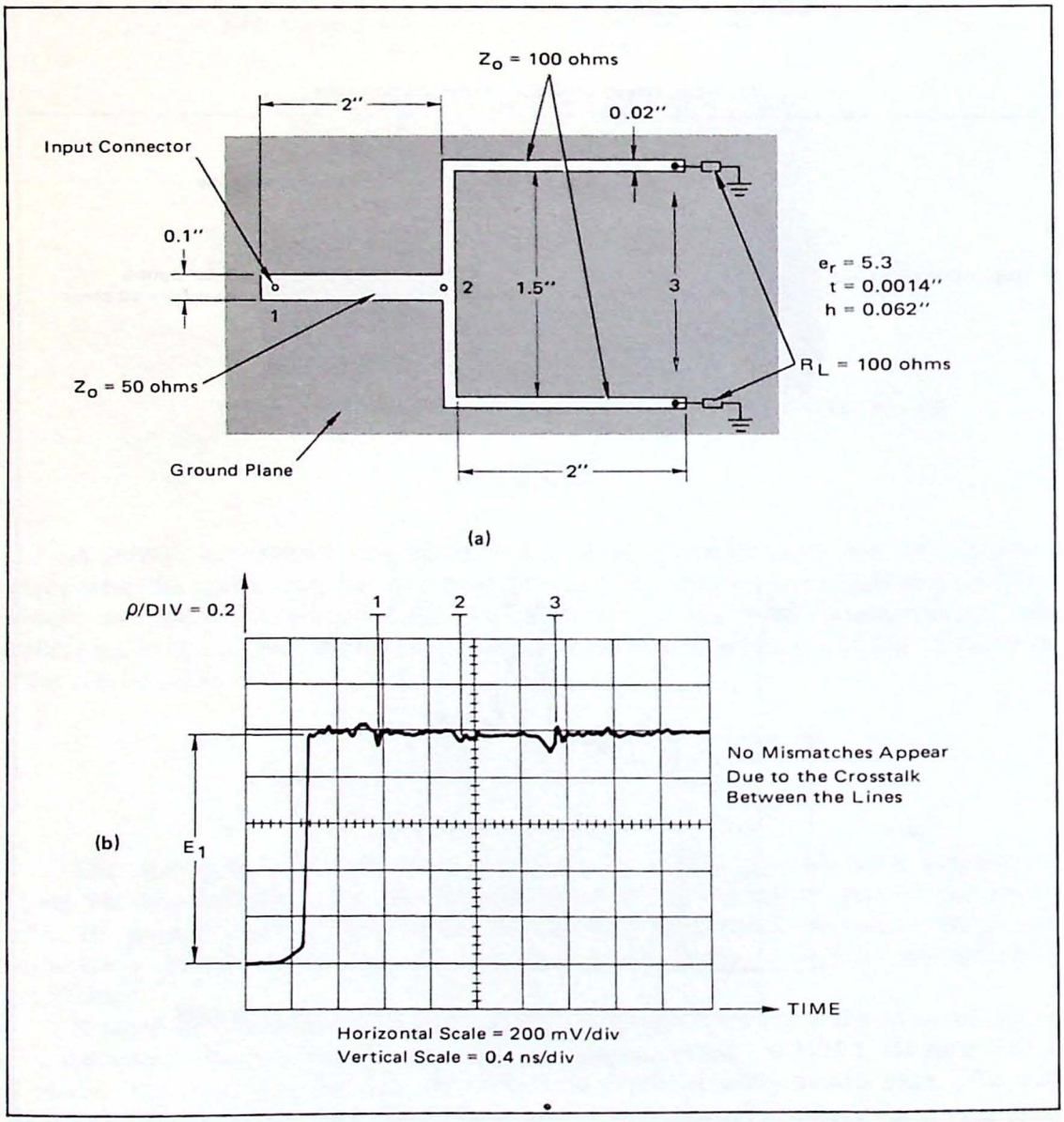
For a discontinuity in the ground plane of 2.5 inches length, a propagation delay of the line of 0.15 ns/in, and a MECL III gate with 1 ns rise time, the percent reflected voltage can be calculated. From Figure 7-13(b), ρ is found to be 0.36. Using equation 23,

$$\rho' = \frac{2(0.36)\,(2.5)\,(0.15)}{(1)} = 0.27 \quad .$$

Therefore, the reflection would be 27%. For a MECL 10,000 series gate, with a rise time of 3.5 ns, the reflection would only be 7.7%.

TDR Example 5. Another measurement was performed, as shown in Figure 7-14, to observe the reflections due to the use of a hybrid divider. The construction of the

7-14: Hybrid Divider

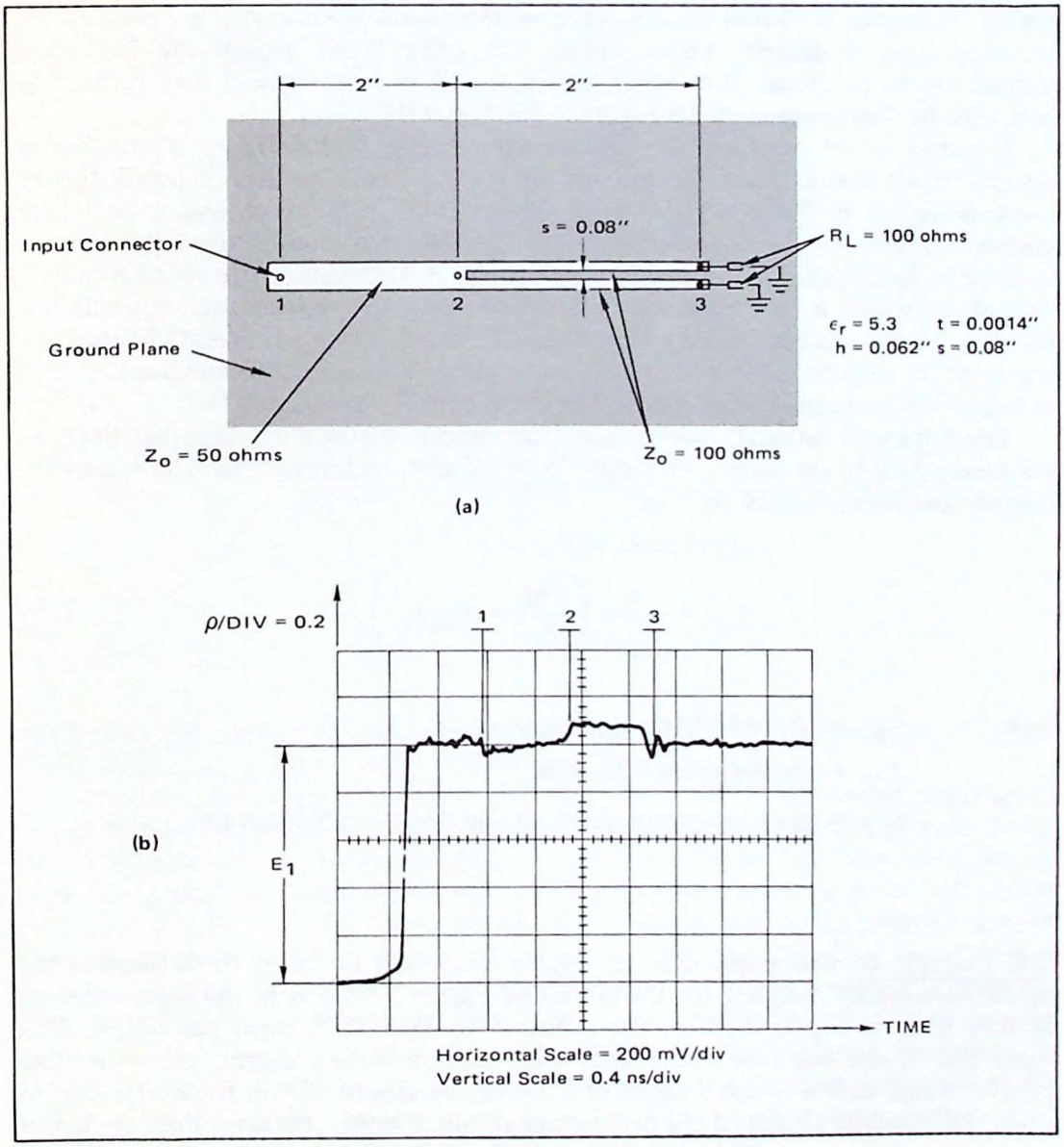


microstrip board used is shown in the figure. Note that the 50 ohm line branches out into two 100 ohm lines. A reflection of 4 percent is observed at point 2 where the junction occurs. Notice that the resistor exhibits a reflection of -8%, due to capacitance of the resistor.

Previously it was found that the 50 ohm resistor was inductive. Both results agree with Reference 8 in which it is stated that the lower values of resistors (<75 Ω) exhibit inductance, while the higher values behave capacitively. These effects are also shown in the data in Figure 4 of Chapter 4. Note that no mismatch appears due to crosstalk between the two 100 ohm branches, because of their wide separation.

Figure 7-15(b) shows the reflection due to the construction of Figure 7-15(a) where the two 100 ohm lines have been brought close together. The reflection at point 2 is now equal to 8% arising from the cross coupling of the two lines. Crosstalk is discussed in References 5, 9, 10, and 11.

7-15: Hybrid Divider With Crosstalk Problem



Even mode or odd mode characteristic impedance (Z_{oe} or Z_{oo}) can be considered to exist in a circuit with crosstalk. One, Z_{oe}, is due to the strips being at the same potential and carrying equal currents in the same direction. The other, Z_{oo}, is due to the strips being at equal but opposite potentials and carrying equal currents in opposite directions. The backward crosstalk voltage, V_B, on a passive line is given in Reference 10 as:

$$V_B = \left(\frac{Z_{oe} - Z_{oo}}{Z_{oe} + Z_{oo}} \right) E_1 \quad , \tag{24}$$

where E_1 is the signal propagating down the active line. Formulas are given in References 9 and 12 for calculating Z_{oe} and Z_{oo}. The backward crosstalk voltage shown in Figure 7-15(b) at point 2 is equal to 8% of the incident voltage E_1. Since both lines are active, the crosstalk due to one active line is 4% of E_1 for a spacing of 80 mils. Reference 5 should be consulted if information concerning crosstalk on microstrip lines is desired. There, curves are given from which the backward crosstalk can be predicted. (For example, Figure 10 in Reference 5 may be used to predict the backward crosstalk for Figure 7-15(a) as 11%).

Crosstalk is not ordinarily a problem when using MECL III on microstrip or strip line circuit boards, when line spacings are greater than 30 mils. Crosstalk theory is well described in Reference 11. In it, the mutual inductance and capacitance between two lines are used to determine the crosstalk coefficient. Crosstalk theory is presented in some detail in this handbook in Chapter 4, "System Interconnections". Forward crosstalk is normally much smaller than the backward crosstalk on microstrip lines – except for very long lines (>5 feet). Forward crosstalk does not exist at all on strip lines, since they are made with a homogeneous medium, so that the inductively and capacitively induced currents cancel (Reference 10).

The backward crosstalk coefficients for various types of microstrip lines on glass epoxy boards are shown in Figure 7-16 (cf also Reference 5). The backward crosstalk coefficient is equal to:

$$K_B = \frac{1}{4t_{pd}} \left(\frac{L_M}{Z_o} + C_M Z_o \right) \quad , \tag{25}$$

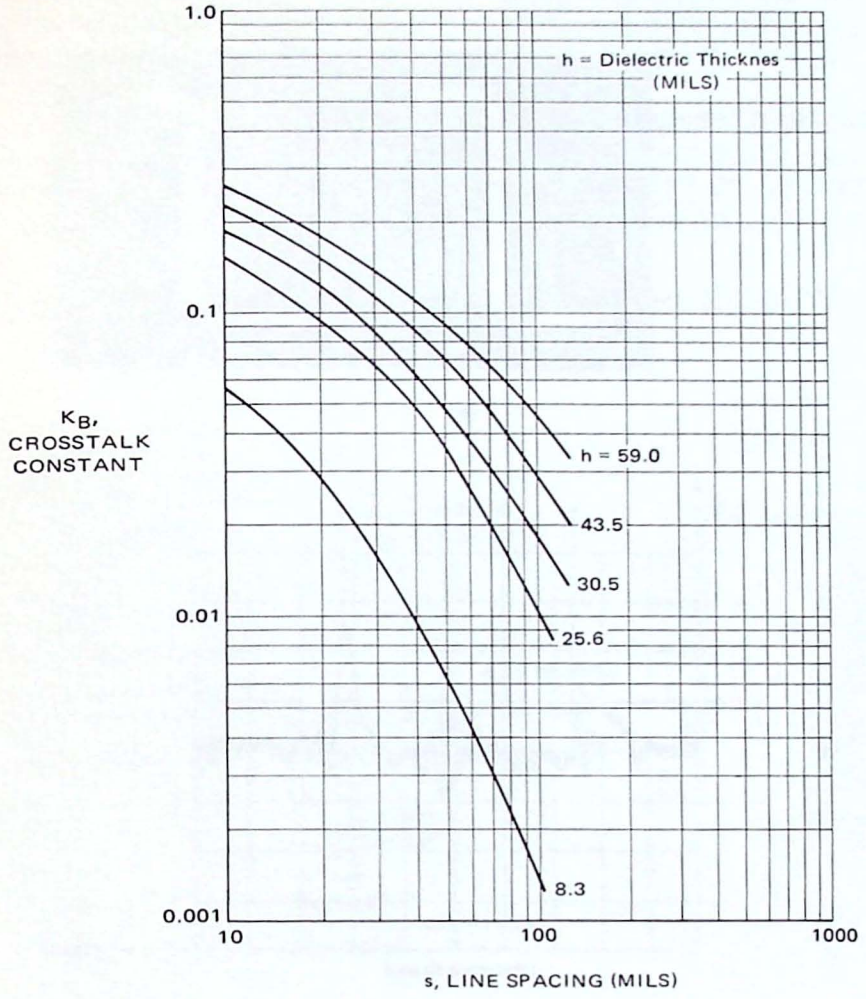
where: L_M = the inductive coupling,

C_M = the capacitive coupling,

t_{pd} = the propagation delay of the line per unit length.

TDR Example 6. The graph data in Figure 7-16 will be used to determine the percent of crosstalk coupling for the circuit of Figure 7-15. From the dimensions of the lines given in Figure 7-15(a), K_B is found to be 0.055 from the graph. This means that if one line (the active line) were driven with a signal, the other line (passive) would have a coupled signal of 5.5% of the amplitude on the active line, in a direction opposite to that of the driving signal. Since both 100 ohm lines are active

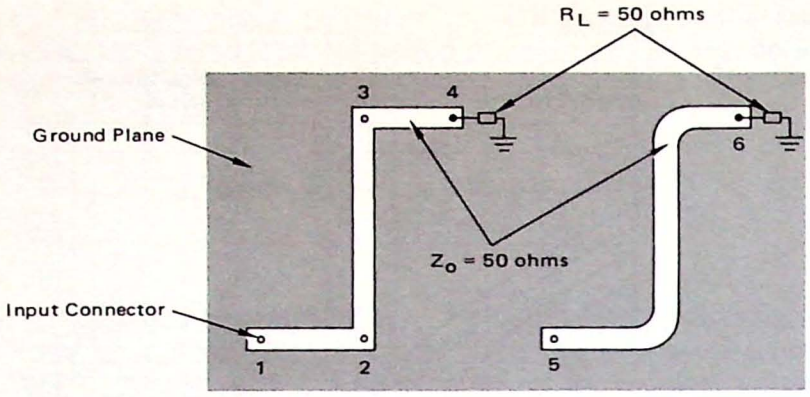
7-16: Backward Crosstalk Coefficient for Microstrip Lines on Glass Epoxy Boards (G-10 Material)



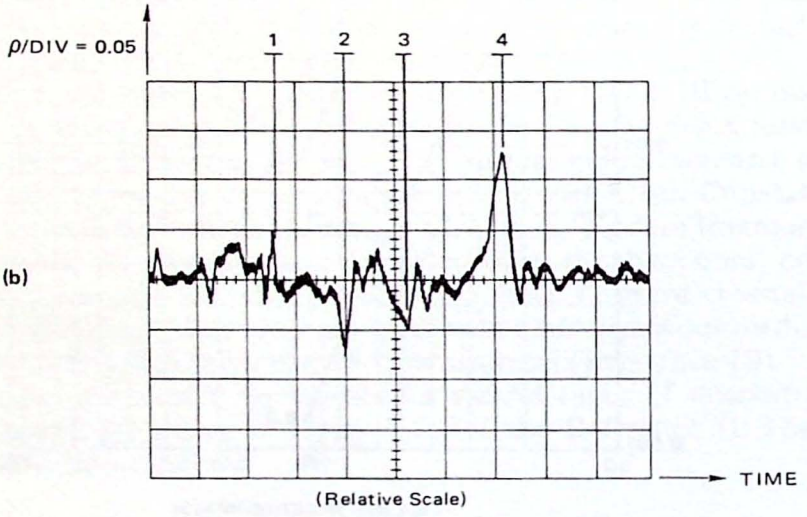
simultaneously, the reflection observed on the TDR is twice as much, or 11%. From Figure 7-15, the actual crosstalk can be seen to be about 8%.

In very high speed systems, the exact shape of a line can be important, if reflections are to be kept to a minimum. The arrangement shown in Figure 7-17(a) has been used to investigate the behavior of two different line shapes. For one line, corners are sharp. This permits the width of the line to be larger at corners than elsewhere. Figure 7-17(b) shows that a −7.5% reflection occurs at point 6 due to the lowered characteristic impedance at the corner. For the other line, the corners are rounded to produce a constant line width. Figure 7-17(c) shows that a constant line impedance exists for the second line. Note that an inductive reflection, as discussed before, does occur at the end of the line due to the inductance of the resistor. In conclusion, it is desirable to have smooth, rounded line edges and constant line widths when designing transmission lines for high speed systems. Resistor leads should be kept short to minimize termination inductance.

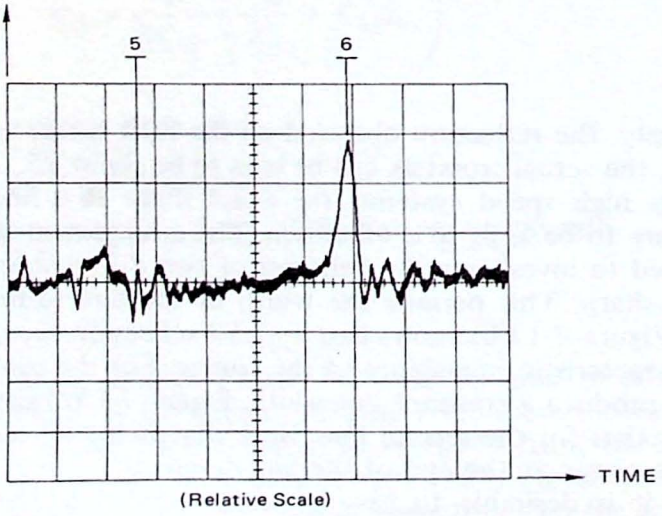
7-17: Reflections Caused by Signal-Line Shape Variations



(a)



(b)



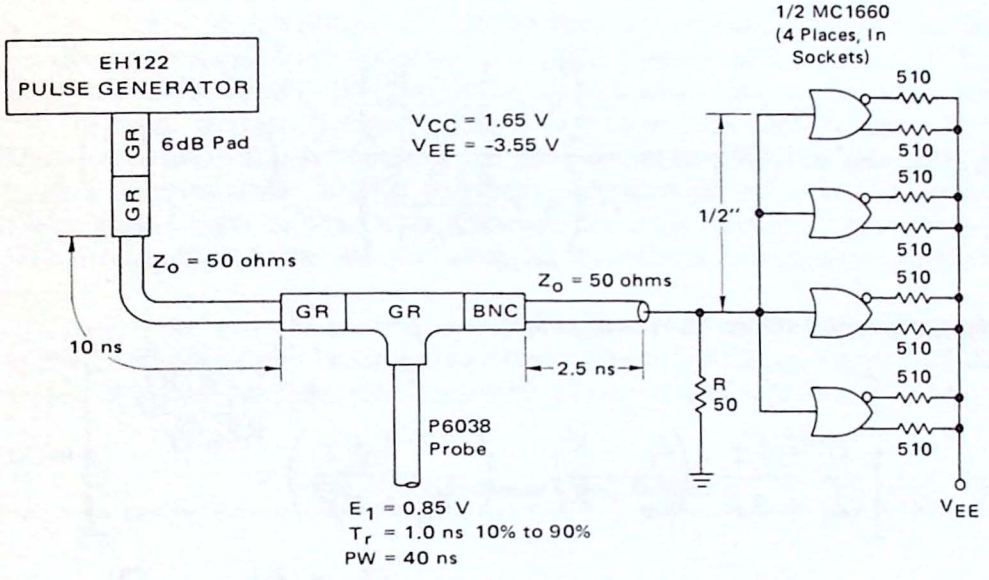
(c)

The Effect of Loading, on a Parallel Terminated Transmission Line

For designing high speed systems it is useful to understand the effects of loading a transmission line with MECL circuit inputs. Some tests were performed to determine the equivalent loading effects of a MECL gate load. The input impedance of the MECL gate is high and may be assumed to be purely capacitive as far as reflections are concerned.

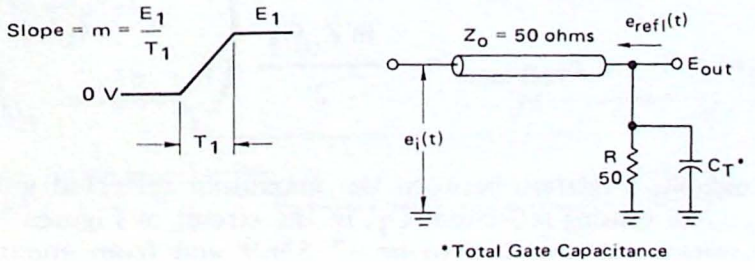
Accurate knowledge of gate input capacitance is necessary to develop accurate loading rules. A test setup, similar to that for a TDR, was used to determine the amount of reflection that occurred when driving four MECL III gates (MC1660L – cf Figure 7-18). The amount of reflection that occurred at the probe was found to

7-18: Test Setup for Measuring the Reflection From Four MECL III Gate Loads



be 275 mV, in a direction indicating it was due to a terminal capacitance, C_T. A formula may be derived so that the amount of this capacitance can be calculated. Figure 7-19 shows the equivalent circuit which will be used for the derivation of

7-19: Circuit for Driving the Maximum Reflected Voltage Due to the Capacitance of the Gate Inputs



such a formula.

The reflection coefficient at the load is:

$$\rho_L(s) = \frac{Z_L - Z_o}{Z_L + Z_o} = \frac{\dfrac{R}{sRC_T + 1} - Z_o}{\dfrac{R}{sRC_T + 1} + Z_o} = \frac{(R - Z_o) - sRZ_oC_T}{(R + Z_o) + sRZ_oC_T} \quad . \tag{26}$$

From equation 18, the LaPlace transform of the input voltage can be found to be:

$$E_i(s) = \frac{m}{s^2}\left(1 - e^{-T_1 s}\right) . \tag{27}$$

The reflected voltage at the load, in LaPlace notation, is:

$$E_{refl}(s) = E_i(s)\rho_L(s) = \frac{-\left(s + \dfrac{Z_o - R}{RZ_oC_T}\right)}{s^2\left(s + \dfrac{Z_o + R}{RZ_oC_T}\right)}\, m\left(1 - e^{-T_1 s}\right) . \tag{28}$$

Taking the inverse LaPlace transform yields:

$$e_{refl}(t) = -\left[\frac{2R^2Z_oC_T}{(Z_o + R)^2} + \left(\frac{Z_o - R}{Z_o + R}\right)t - \left(\frac{2R^2Z_oC_T}{(Z_o + R)^2}\right)e^{-\frac{(Z_o + R)}{RZ_oC_T}t}\right] mU(t) +$$

$$\left[\frac{2R^2Z_oC_T}{(Z_o + R)^2} + \left(\frac{Z_o - R}{Z_o + R}\right)(t - T_1) - \left(\frac{2R^2Z_oC_T}{(Z_o + R)^2}\right)e^{-\frac{(Z_o + R)}{RZ_oC_T}(t - T_1)}\right] mU(t - T_1) . \tag{29}$$

The maximum reflection occurs at $t = T_1$. Then for $R = Z_o$, we obtain:

$$e_{refl}(t = T_1) = E_{refl\,max} = -\frac{m\,Z_oC_T}{2}\left(1 - e^{-\frac{2T_1}{Z_oC_T}}\right) \tag{30}$$

Equation 30 exhibits a relation between the maximum reflected voltage and the effective capacitance causing reflection, C_T, in the circuit of Figures 7-18 and 7-19. The reflected voltage was measured to be -275 mV and from equation 22, T_1 is found to be 1.25 ns. Thus the total capacitance, obtained from equation 30, is C_T = 17.2 pF. Since stray capacitance, C_s, is approximately 4.0 pF, the capacitance

due to the gate loads is the difference between C_T and C_S i.e., 13.2 pF, or 3.3 pF per gate input.

For comparison, an RF vector impedance meter was used to measure the input capacitance of a similar 4 gate setup at a frequency of 50 MHz. The total capacitance measured 20 pF. Since the stray capacitance for this configuration measured 6.5 pF, the capacitance due to the four gate loads is 13.5 pF, or 3.38 pF per gate input. It is felt that the two methods agreed well enough with each other to say that the equivalent load of a MECL III input is 3.3 pF.

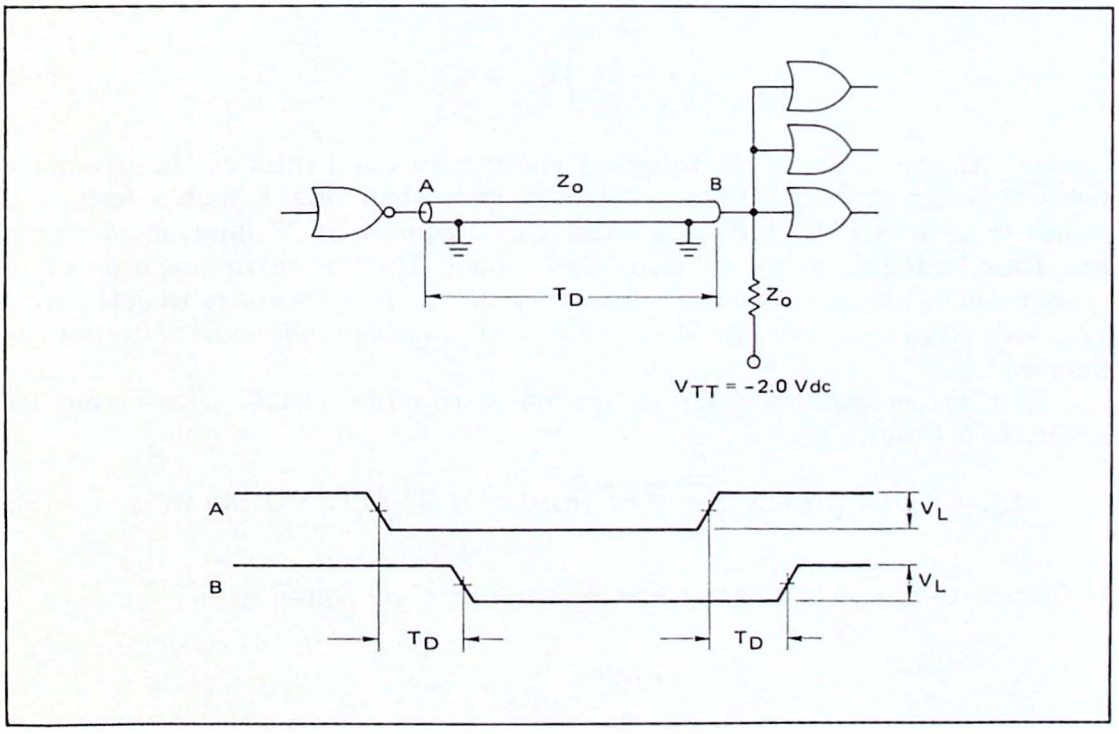
MECL 10,000 series elements were also tested. It was found that a MECL 10,000 gate input measured 2.9 pF using the RF vector impedance meter. Using the reflection method of Figure 7-18 and equation 30, the capacitance of a gate input was found to be 2.7 pF.

If printed circuit cards are used without sockets, 3.3 pF per MECL III gate input and 2.9 pF per MECL 10,000 gate input should be used. These values will be used in later calculations.

It was shown in equations 12 and 13 that the maximum length of an unterminated line (stub length) is a function of loading. Figures 3-13, 3-14, and 3-15 are a tabulation of some values of permissible lengths versus fanout and logic family. However, in most designs it becomes necessary to increase the line length beyond the distances specified in the table. It has been shown that for long lines, $2T_D$ (line) $> t_r$ (pulse), a termination resistor will reduce or eliminate reflections. In a practical situation, a MECL gate driving a transmission line must feed other gates along that line. So it is important to be able to determine the effects of individual gate loads on the line.

There are two ways of placing gates on a parallel terminated transmission line: one is called "distributed" loading, the other "lumped" loading. Figure 7-20 shows an example of a parallel terminated line with a lumped load at the end. The term T_D

7-20: Driving a Parallel Terminated Line



represents the delay of the line. Since a full logic swing is available all along the line, parallel termination permits distributed loading to be placed anywhere along the line.

The change in characteristic impedance of a line caused by gate loads being distributed along the line can be calculated. For a lossless line the characteristic impedance of a transmission line is:

$$Z_o = \sqrt{\frac{L_o}{C_o}} \quad , \tag{31}$$

where L_o is the intrinsic inductance of the line and C_o is the intrinsic capacitance of the line, both per unit length. The MECL gate has a high input impedance so that only the capacitive effect need be considered for ac conditions. The characteristic impedance of a transmission line altered by gate loading, Z'_o, is:

$$Z'_o = \sqrt{\frac{L_o}{C_o + C_d}} = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} \quad , \tag{32}$$

where Z_o is the original line impedance defined in equation 31 and C_d is the distributed gate capacitance. The propagation delay per unit length of a lossless transmission line is:

$$t_{pd} = \sqrt{L_o C_o} \quad . \tag{33}$$

Rearranging, and using equation 31 gives:

$$t_{pd} = \left(\sqrt{\frac{L_o}{C_o}}\right) C_o = Z_o C_o \quad . \tag{34}$$

Example. An application of the foregoing relationships and rules can be seen in the following design problem. Given: a 68 ohm microstrip line 8 inches long. It is desired to drive four MECL III gate loads spaced equally at 2" intervals along this line. These loads are, of course, "distributed" loads. The microstrip line is on a glass epoxy board which has a dielectric constant, e_r, of 5.0. It is necessary to determine a value for a parallel terminating resistor which will essentially eliminate reflections on the line.

First, the propagation delay of the microstrip line can be found using the relation from Chapter 3:

$$t_{pd} = 1.017 \sqrt{0.475\, e_r + 0.67} \text{ ns/ft} = 1.77 \text{ ns.ft} = 0.148 \text{ ns/in} \quad , \tag{35}$$

in this case. Using equation 34, the line capacitance, C_o is found to be:

$$C_o = \frac{0.148}{68} = 2.18 \text{ pF/in.}$$

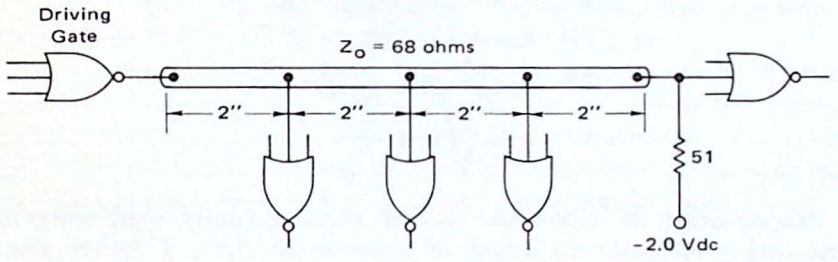
Four MECL III gate loads are equivalent to a load capacitance of 13.2 pF which is distributed along 8 inches of line. Therefore, C_d = 13.2 pF/8 in. = 1.65 pF/in. Substituting these values into equation 32 gives:

$$Z'_o = \frac{68}{\sqrt{1 + \frac{1.65}{2.18}}} = 51.5 \text{ ohms.}$$

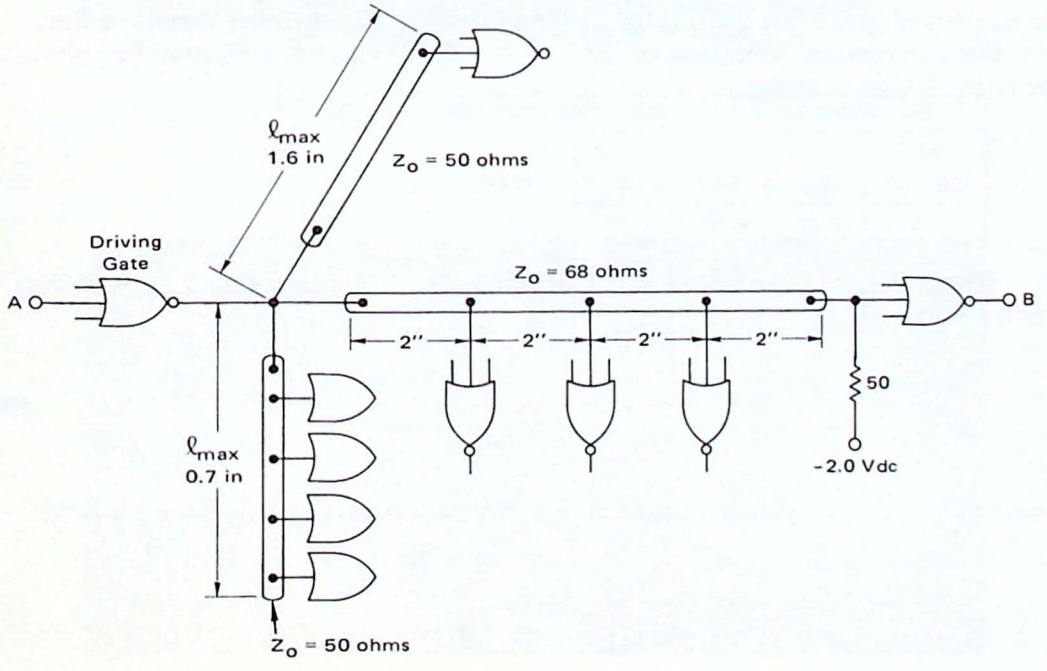
Thus, a 51 ohm termination resistor would be acceptable for terminating the 8 inch 68 ohm microstrip line with four distributed MECL III gates. The resulting circuit is shown in Figure 7-21.

The driving gate shown in Figure 7-21, besides driving the long transmission line, can also drive many lines (no limit) as long as the length of each stub does not exceed the limits of Figures 3-13, 3-14, or 3-15. For instance, if a 50 ohm microstrip line were used with MECL III to connect the driving gate to 1 gate load in one direction, and to four gate loads in another direction (in addition to the loads shown in Figure 7-21), then from Figure 3-15 the maximum permissible stub lengths are 1.6 and 0.7 inches, respectively (of Figure 7-22). It should be noted that the four

7-21: Example Illustrating Distributed Loading



7-22: MECL III Gate Driving a Long Transmission Line with Distributed Loads, and Short Stubs at the Driving Source



gates on the stub (ℓ_{max} = 0.7 inch) could be lumped at the end of that line, without the need for any other changes.

In order to determine the amount of reflection which can be tolerated on a line, the following development is presented. Reflection is, of course, caused by gate loading which produces a change in the impedance on a section of the transmission line. The equations to be developed use distributed line theory – an approximate method, but one which gives very accurate results, as verified in Reference 11.

The reflection coefficient given in equation 3 can be revised to take into account the reflection due to the altered characteristic impedance produced by loading:

$$\rho = \frac{Z'_o - Z_o}{Z'_o + Z_o} .$$

Substituting the expression for Z'_o given in equation 32 yields:

$$\rho = \frac{1 - \sqrt{1 + \frac{C_d}{C_o}}}{1 + \sqrt{1 + \frac{C_d}{C_o}}} . \tag{36}$$

From this equation, it is possible to find the maximum load capacitance that can be distributed or lumped on a length of transmission line. Further, the length of transmission line for distributing loads will be assumed to be the stub length defined in equations 12 and 13. This length of line will limit reflection discontinuities caused by differences between distributed and lumped loads. However a rule is needed which can be stated for a particular value of transmission line, to specify a limit for the number of gate loads distributed or lumped along an arbitrary length of line.

For a maximum reflection of 20% (ρ = -0.20) equation 36 may be solved for the ratio of C_d/C_o, giving:

$$\frac{C_d}{C_o} = 1.25 . \tag{37}$$

Since C_d is the distributed gate load capacitance per unit line length, it may be written that:

$$C_d = \frac{C_D}{\ell_{max}} , \tag{38}$$

where C_D is the total gate load capacitance. Substituting into equation 37 yields:

$$\frac{C_D}{C_o} = 1.25\ \ell_{max} . \tag{39}$$

For a 50 ohm microstrip transmission line, on a glass epoxy board, with MECL III gates, with C_O = 2.96 pF/in, and t_r = 1.1 ns, equation 12 may be used to find $\ell_{max} \approx 2.5$ inches. Then substituting into equation 39 and solving: C_D = 9.2 pF. This means that up to 9.2 pF can be distributed or lumped along any 2.5 inches of 50 ohm microstrip line using MECL III. Two MECL III gate loads can be used along any 1.8 inches of line for a carefully laid out board, or two MECL III gate loads and 2.6 pF of stray capacitance can be distributed or lumped along any 2.5 inches of line.

For a 50 ohm strip line on a glass epoxy board and using MECL III gates, with C_O = 3.77 pF/in and t_r = 1.1 ns, equations 13 and 39 may be used to find $\ell_{max} \approx 2.0$ inches. Then substituting into equation 39 and solving, C_D = 9.4 pF. This means that up to 9.4 pF can be distributed or lumped along any 2.0 inch portion of 50 ohm strip line when using MECL III gates. If 3.3 pF per gate input is used, then from equation 39 two gate loads can be lumped or distributed along any 1.4 inch portion of a 50 ohm strip line.

It is seen from these calculations that strip line has an advantage over microstrip: it can be used for driving more gate loads per unit length than microstrip, granting the same amount of reflection in each case. This is due to strip line having a larger capacitance per unit length. Figure 7-23 gives values for the maximum capacitance that can be lumped or distributed over any length (ℓ_{max}) of line for MECL III, MECL 10,000, and high speed MECL II.

As an example of how Figure 7-23 can be used, suppose 68 ohm microstrip lines are to be used with the MECL 10,000 series. From the Figure, 21 pF of capacitance of five gate loads can be lumped or distributed over any 7.7 inch portion of the line. The rise times shown in the figure are characteristic of the particular logic family and were used in the calculations to obtain the data.

7-23: Maximum Capacitance That Can Be Lumped or Distributed Over a Length of Terminated Transmission Line ℓ_{max}.

	CHARACTERISTIC IMPEDANCE OF TRANSMISSION LINE						
	STRIPLINE (e_r = 5.0)			MICROSTRIP (e_r = 5.0)			COAX (e_r = 2.2)
	50 Ω	68 Ω	90 Ω	50 Ω	68 Ω	90 Ω	50 Ω
MECL III							
C_{max} (pF)	9.4	6.9	5.2	9.2	6.8	5.1	9.4
ℓ_{max} (in)	2.0	2.0	2.0	2.5	2.5	2.5	3.0
t_r (ns) = 1.1							
MECL 10,000							
C_{max} (pF)	29	21.5	16.2	28.6	21	15.9	29
ℓ_{max} (in)	6.2	6.2	6.2	7.7	7.7	7.7	9.3
t_r (ns) = 3.5							
MECL II½							
C_{max} (pF)	16.4	12.0	9.1	16.2	11.9	9.0	16.5
ℓ_{max} (in)	3.5	3.5	3.5	4.4	4.4	4.4	5.3
t_r (ns) = 2.0							

Analysis: Series Terminated Lines Compared to Parallel Terminated Lines

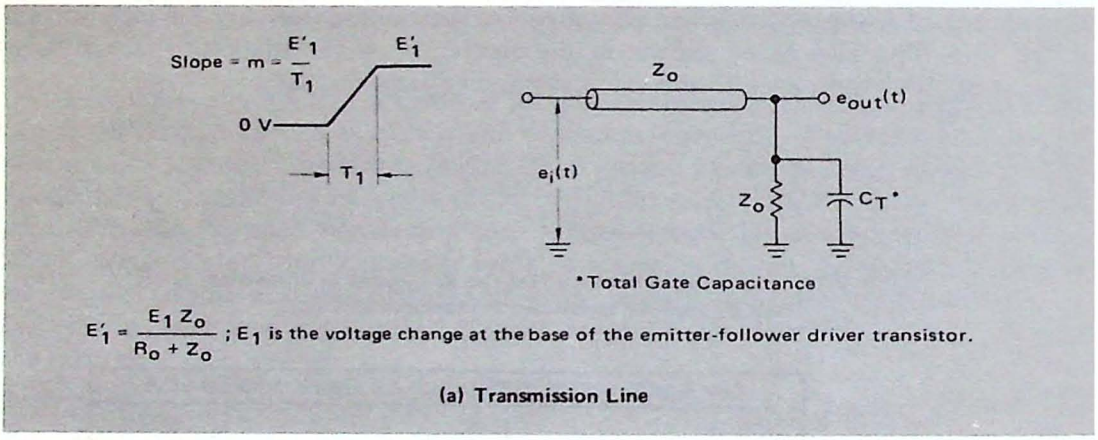
The propagation delay increase due to gate loading when a line is series terminated is about twice as large as for a comparable parallel terminated line. Equation 11 gives a fairly close approximation for the propagation delay of a parallel terminated line with loading. This equation was:

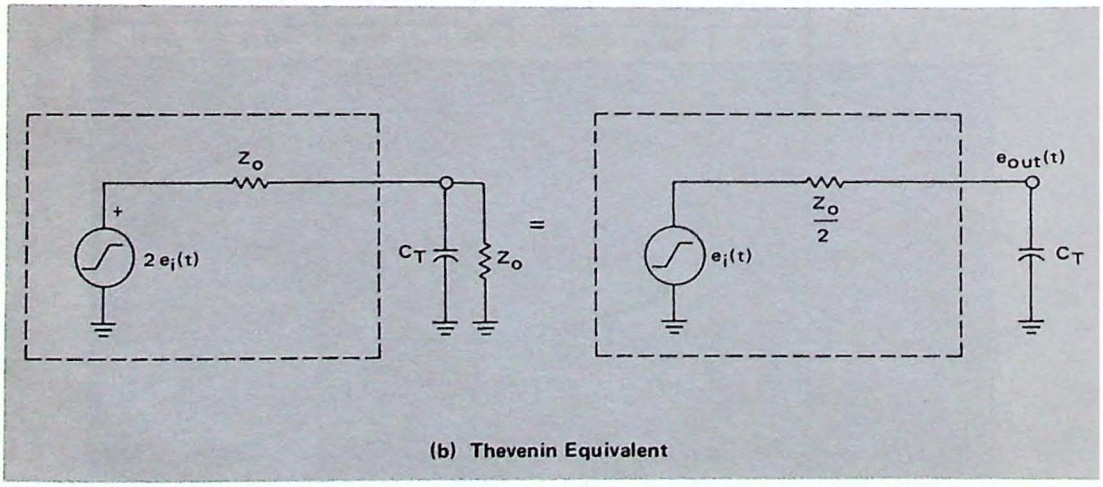
$$t'_{pd} = t_{pd}\sqrt{1 + \frac{C_d}{C_o}} \quad . \tag{11}$$

The output waveform at the end of a series terminated line or at the end of a parallel terminated line can be derived from an equivalent circuit using Thevenin's Theorem, assuming the line is long ($2T_D >> t_r$). Figure 7-24(a) shows a parallel terminated transmission line circuit, along with the waveform driving the line.

The equivalent open circuit voltage of the line is twice the input voltage and the Thevenin resistance is the impedance of the open line at the load looking toward the source. The Thevenin equivalent for a parallel terminated line is shown in Figure

7-24: Parallel Terminated Transmission Line, and its Thevenin Equivalent



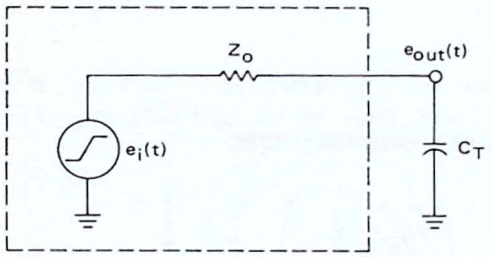


7-24(b). Figure 7-25 shows the Thevenin equivalent for a series terminated line. Note that the impedance (Z_o) of the series terminated line is twice as large as that for the parallel terminated line. A general equation can be derived for the output voltage assuming the impedance in the circuit to be R. Then a substitution for R will give the equations for both types of lines.

Writing the equation around either Thevenin equivalent loop:

$$e_i(t) = iR + \frac{1}{C_T} \int_o^t i \, dt \quad . \tag{40}$$

7-25: Thevenin Equivalent of Series Terminated Transmission Line



But also:

$$e_i(t) = mt\,U(t) - m(t - T_1)\,U(t - T_1) \quad . \tag{41}$$

Equating the equations and taking the LaPlace transform of both sides gives:

$$\frac{m}{s^2} - \frac{m}{s^2} e^{-T_1 s} = RI(s) + \frac{I(s)}{C_T s} = \left(R + \frac{1}{C_T s} \right) I(s) \quad . \tag{42}$$

But:

$$e_{out}(t) = \frac{1}{C_T} \int_o^t idt \quad \text{or} \quad E_{out}(s) = \frac{I(s)}{C_T s} \quad . \tag{43}$$

Therefore:

$$\frac{m}{s^2} - \frac{m}{s^2} e^{-T_1 s} = \left(R + \frac{1}{C_T s} \right) C_T s \, E_{out}(s) \quad . \tag{44}$$

Solving for $E_{out}(s)$:

$$E_{out}(s) = \frac{\frac{m}{s^2}\left(1 - e^{-T_1 s}\right)}{C_T s\left(R + \frac{1}{C_T s}\right)}, \tag{45}$$

which reduces to:

$$E_{out}(s) = \frac{\frac{m}{RC_T}\left(1 - e^{-T_1 s}\right)}{s^2\left(s + \frac{1}{RC_T}\right)} . \tag{46}$$

Taking the inverse LaPlace transform yields:

$$e_{out}(t) = \left[mRC_T\left(e^{\frac{-t}{RC_T}} - 1\right) + mt\right] U(t) - \left[mRC_T\left(e^{\frac{-(t - T_1)}{RC_T}} - 1\right) + m(t - T_1)\right] U(t - T_1) . \tag{47}$$

Equation 47 defines the output voltage for a series terminated transmission line when $R = Z_o$; it defines the output voltage for a parallel terminated transmission line when $R = Z_o/2$.

From equation 47 the equation for the series terminated line can be written:

$$e_{out}(t) = \frac{E'_1 Z_o C_T}{T_1}\left(e^{\frac{-t}{Z_o C_T}} - 1\right) + \frac{E'_1}{T_1}(t) \quad \text{for } t \leq T_1 , \tag{48}$$

and:

$$e_{out}(t) = \frac{E'_1}{T_1} Z_o C_T \left(1 - e^{\frac{T_1}{Z_o C_T}}\right) e^{\frac{-t}{Z_o C_T}} + E'_1 \quad \text{for } t > T_1 , \tag{49}$$

where E'_1 is defined in Figure 7-24. The equations for the parallel terminated line can also be written:

$$e_{out}(t) = \frac{E'_1 Z_o C_T}{2T_1}\left(e^{\frac{-2t}{Z_o C_T}} - 1\right) + \frac{E'_1}{T_1}(t) \quad \text{for } t \leq T_1 . \qquad (50)$$

and:

$$e_{out}(t) = \frac{E'_1 Z_o C_T}{2T_1}\left(1 - e^{\frac{2T_1}{Z_o C_T}}\right) e^{\frac{-2t}{Z_o C_T}} + E'_1 \quad \text{for } t > T_1 . \qquad (51)$$

If the input voltage is assumed to be a step function, then the equation for the output voltage for a series terminated line can be written as:

$$e_{out}(t) = E'_1\left(1 - e^{\frac{-t}{Z_o C_T}}\right) , \qquad (52)$$

and for a parallel terminated line:

$$e_{out}(t) = E'_1\left(1 - e^{\frac{-2t}{Z_o C_T}}\right) . \qquad (53)$$

To derive the equation for the additional propagation delay due to gate loading at the end of the line, equations 52 and 53 will be used. A more exact equation can be derived using equations 48 through 51 but the analysis is more difficult due to the complexity of the equations. Letting $e_{out}(t) = 0.5\, E'_1$ and solving for t, we obtain a propagation delay time of:

$$t_{pd} = 0.7\, Z_o C_T \quad \text{for series termination,} \qquad (54)$$

and:

$$t_{pd} = 0.35\, Z_o C_T \quad \text{for parallel termination.} \qquad (55)$$

These additional line delays should be added to the existing physical line delay as expressed in equation 34 to obtain total system line delay. To derive the equation

for the output rise time, t_{ro}, knowing the input rise time, t_{ri}, equations 49 and 51 will be used. The output rise time is defined as the time it takes for the output voltage to travel from 10 to 90% of its final value. T_1 is defined as:

$$T_1 \approx 1.2\, t_{ri} \ . \tag{56}$$

Substituting into Equation 49, rearranging, and taking the natural log of both sides, the output rise time at the end of the transmission line is obtained:

$$t_{ro} = Z_o C_T \ln \left[\frac{Z_o C_T}{0.18\, t_{ri}} \left(\frac{1.2 t_{ri}}{e^{Z_o C_T}} - 1 \right) \right], \quad \text{for series termination.} \tag{57}$$

Doing the same thing with equation 51:

$$t_{ro} = \frac{Z_o C_T}{2} \ln \left[\frac{Z_o C_T}{0.36\, t_{ri}} \left(\frac{2.4 t_{ri}}{e^{Z_o C_T}} - 1 \right) \right], \quad \text{for parallel termination.} \tag{58}$$

Equations 56 and 57 may also be used to solve for the output fall time by substituting the input fall time, t_{fi}, in place of t_{ri}.

Example. An example will be shown to illustrate the use of equations 54 through 58 using MECL 10,000 gates. Figure 7-26(a) and (b) shows comparable setups for series and parallel termination. The load gates at point B were placed in sockets. The total capacitance at point B is C_T = 20 pF which takes into account the gate capacitances, socket capacitance, as well as interconnect and stray capacitances. The propagation delay due to the transmission line from A to B is 1.75 ns. The rise and fall times at point A, due to the MECL 10,000 driving gate, are t_{ri} = 3.5 ns, and t_{fi} = 2.8 ns. From equation 54, the propagation delay increase due to the series termination is: (0.7) (50 ohms) (20 pF) = 0.7 ns. From equation 55, the propagation delay due to the parallel terminations is half as much, 0.35 ns. Therefore, the total propagation delay from point A to B is 2.45 ns for series termination, and 2.1 ns for parallel termination.

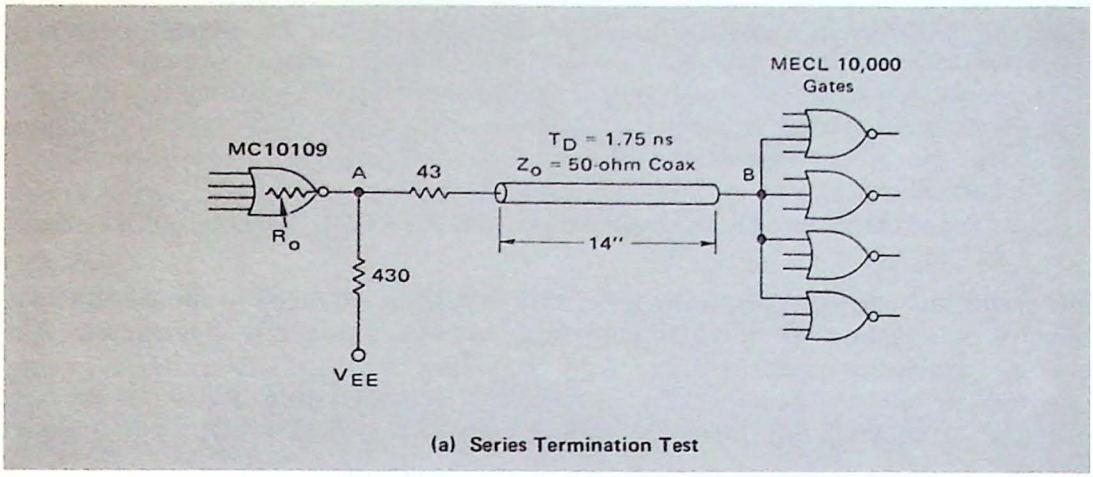
The rise and fall times at point B can be calculated from equations 56, 57, and 58. The mathematical 10 to 90% rise time at point B is 4.65 ns for series termination, versus 4.1 ns for parallel termination. The fall time at point B is 4 ns for series termination versus 3.35 ns for parallel termination. Measured test results agreed closely with the calculated values.

Equation 11 could have been used to calculate the propagation delay from A to B for the parallel termination arrangement. Solving for t'_{pd}:

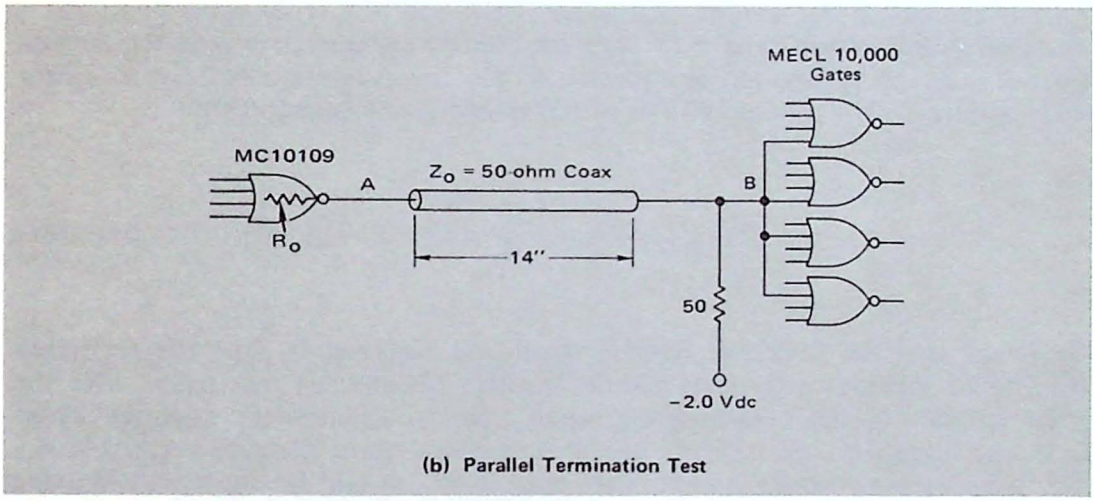
$$t'_{pd} = 1.75 \text{ ns} \sqrt{1 + \frac{20 \text{ pF}}{35 \text{ pF}}} = 2.2 \text{ ns} \ ,$$

which is very close to the value of 2.1 ns that was calculated using equation 54.

7-26: Test Setups for Comparison of Propagation Delays from A to B, and the Rise and Fall Times at B



(a) Series Termination Test



(b) Parallel Termination Test

Since the propagation delay increase is twice as much for a series terminated line as for a parallel terminated line, an equation similar to equation 11 can be derived. The propagation delay of a series terminated line can be written as:

$$t'_{pd} = t_{pd}\left[2\left(\sqrt{1+\frac{C_T}{C_o}}-1\right)+1\right], \qquad (59)$$

where t'_{pd} is the modified propagation delay of the line, t_{pd} is the original propagation delay of the line, C_T is the total capacitance at the end of the line, and C_o is the intrinsic capacitance of the transmission line.

The effective characteristic impedance of a transmission line decreases with capacitance at the end of the series terminated line, but only half as much as for a parallel terminated line (cf equation 32). The characteristic impedance due to

loading of a series terminated transmission line can be written:

$$Z'_o = \frac{2 Z_o}{\sqrt{1 + \frac{C_T}{C_o}} + 1} = R_S + R_o \qquad (60)$$

This means that the series terminating resistor should be changed in the proportion indicated by equation 60 when the capacitance at the end of the line exceeds the value of capacitance given in Table 7-23. Equation 60 has been verified in the laboratory as valid for heavy loading conditions. If the resistor, R_S, is not altered according to equation 60, increased propagation delays will result from underdamping.

Furthermore, if the amount of loading at the end of a series terminated line is more than that shown in Table 7-23, then the emitter pulldown resistor, R_E, should be lower than the value given in equation 61 for the maximum pulldown resistor value (Chapter 3). The maximum value of R_E as stated in Chapter 3 is:

$$R_{E(max)} = \frac{10 Z_o - R_S}{n} . \qquad (61)$$

The reason that the pulldown resistor should be lowered is that the reflection returning to the source contains a short positive component associated with the slower fall rate of the negative-going signal (due to capacitance loading). Thus, the output transistor will turn off due to this momentary positive reflection if a value given by equation 61 is used. The value of R_E should be chosen so that the output transistor of the driving gate is furnishing enough current to supply the maximum reflection without switching off. The maximum reflection on a series terminated line, due to capacitance, is +0.4 volts. Therefore, the value of R_E should be reduced enough so that the output transistor will be able to supply an additional current of $0.4/Z_o$. A modified emitter pulldown resistor equation can be written as:

$$R'_{E(max)} = \frac{3.6}{\frac{3.6}{R_{E\,max}} + \frac{0.4}{Z_o}} , \qquad (62)$$

where $R_{E\,(max)}$ is defined in equation 61.

There is no limit (due to reflections) on the amount of gate loading that can be placed at the end of a series terminated line, as long as equation 60 is used to determine the proper series terminating resistor. All reflections will be terminated at the driving end if the proper value of R_E is chosen with equation 61 or 62. This is true even though the amount of reflection is twice as much for a series terminated line as it is for a parallel terminated one.

The maximum loading for a parallel terminated transmission line is defined in Figure 7-23. There is no limit to the amount of distributed loading that can be placed on the line, as long as equation 32 is used to choose the terminating resistor. In actual practice, there seems to be no limit to the amount of lumped loading that is placed at the end of a parallel terminated line as long as the terminating resistor is chosen this way. This is true as long as there are no other gates stubbed off the line.

For reference purposes, the equations for the reflection that is sent back to the driving source, with lumped loading at the end of either a series terminated line or a parallel terminated line, can be derived from equations 48 and 50 as follows:

$$\text{percent of maximum reflection} = \frac{e_{out}(t) - E'_1}{E'_1} \qquad \text{at } t = T_1 \quad . \quad (63)$$

Therefore, the maximum reflection due to lumped loading at the end of a series terminated line is:

$$\text{percent of maximum reflection} = \frac{Z_o C_T}{T_1} \left(e^{-\frac{T_1}{Z_o C_T}} - 1 \right) \quad , \quad (64)$$

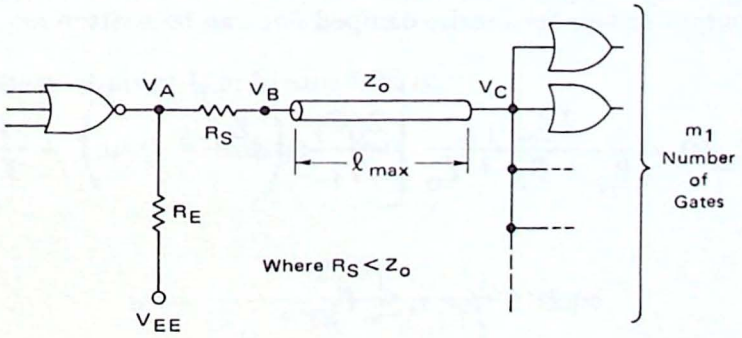
and for lumped loading at the end of a parallel terminated line:

$$\text{percent of maximum reflection} = \frac{Z_o C_T}{2T_1} \left(e^{\frac{-2T_1}{Z_o C_T}} - 1 \right) \quad . \quad (65)$$

Analysis of Series Damping Terminations

A series damped line is very similar to a series terminated line with the exceptions being the line length and the value of the series damping resistor, R_S. The resistor is normally much smaller than the characteristic impedance of the line, Z_o. If $R_S = 0$, then an open line exists for which the maximum length is defined in Figures 3-13, 3-14, or 3-15. If a small value resistor, R_S, is placed in the line, a longer line length is possible. An example of series damping is shown in Figure 7-27

7-27: Series Damping Termination



where the voltage change at point B is defined in Chapter 3 as,

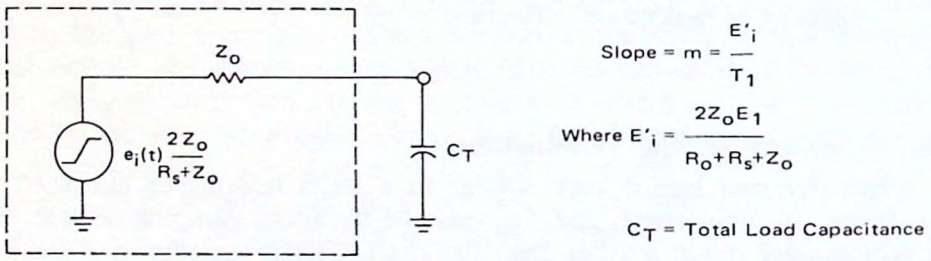
$$\Delta V_B = \Delta V_{INT} \cdot \frac{Z_o}{R_S + R_o + Z_o} \quad . \tag{66}$$

Series damping is primarily used where the characteristic impedance varies – as in backplane wiring when line lengths must be longer than those specified in Figures 3-13 through 3-15. A disadvantage of series damping is that distributed loading cannot be used. A propagation delay slightly slower than for parallel termination also results. Parallel fanout can be used as shown in Figure 3-18.

Figures 3-22, and 3-23, described in Chapter 3, show the minimum values for R_S for any line length, corresponding to specified limits of undershoot and overshoot. These figures were generated by a computer program based on the equations and calculations presented in the following pages. These calculations show how the output voltage from series-damped transmission lines may be derived.

The Thevenin equivalent circuit for a series damped transmission line is shown in Figure 7-28. Note that the circuit is similar to the equivalent circuit for a series terminated line except for the amplitude of the voltage waveform.

7-28: Thevenin Equivalent of a Series Damped Transmission Line



The equations for the output voltage from a series terminated line were derived previously (equations 48 and 49). Since the amplitude has been modified by the factor $(2Z_o/R_o + R_S + Z_o)$, a simple substitution will define the output voltage at the load. The output voltage for a series damped line can be written as:

$$e_{out}(t) = \frac{2Z_oE_1}{R_o + R_S + Z_o}\left[\frac{Z_oC_T}{T_1}\left(e^{\frac{-t}{Z_oC_T}} - 1\right) + \frac{t}{T_1}\right]$$

$$\text{for } t \leq T_1 \ , \tag{67}$$

and:

$$e_{out}(t) = \frac{2 Z_o E_1}{R_o + R_S + Z_o}\left[\frac{Z_o C_T}{T_1}\left(1 - e^{\frac{T_1}{Z_o C_T}}\right)e^{\frac{-t}{Z_o C_T}} + 1\right]$$

$$\text{for } t > T_1 \ , \tag{68}$$

where E_1 is the voltage change at the base of the output emitter follower in the driving gate.

If the input voltage is assumed to be a step function, the equation for the output voltage from a series damped line becomes:

$$e_{out}(t) = \frac{2Z_o E_1}{R_o + R_S + Z_o}\left(1 - e^{\frac{-t}{Z_o C_T}}\right). \tag{69}$$

The additional propagation delay due to gate loading can be found by using equation 69, letting $e_{out}(t) = 0.5\, E_1$, and then solving for t. The increase in the line propagation delay which results, is:

$$t_{pd} = - Z_o C_T \ln\left(\frac{3Z_o - R_S - R_o}{4Z_o}\right). \tag{70}$$

The exact reflected voltage will now be derived by a method similar to that used previously in deriving equation 19. The reflection coefficient at the load is:

$$\rho_L(s) = \frac{\frac{1}{sC_T} - Z_o}{\frac{1}{sC_T} + Z_o} = \frac{1 - sC_T Z_o}{1 + sC_T Z_o} = \frac{-\left(s - \frac{1}{Z_o C_T}\right)}{s + \frac{1}{Z_o C_T}} \ . \tag{71}$$

The input voltage at point B in Figure 7-27 is:

$$e_i(t) = mtU(t) - m(t - T_1)\,U(t - T_1) \ , \tag{72}$$

where:

$$m = \frac{Z_o E_1}{(R_o + R_S + Z_o)\,T_1} = \text{slope} \ .$$

Here R_o is the output impedance of the driving gate; R_S is the series damping resistor; Z_o is the characteristic impedance of the transmission line; E_1 is the voltage change at the base of the output emitter follower of the gate at point A in Figure 7-27; and $T_1 = 1.2\ t_r$ where t_r is the 10 to 90% rise time of the voltage at point A.

Taking the LaPlace transform of equation 72 gives:

$$E_i(s) = \frac{m}{s^2}\left(1 - e^{-T_1 s}\right) . \tag{73}$$

The first reflected voltage waveform at the load at time T_D (point C in Figure 7-27) due to the input voltage is (in LaPlace notation):

$$E_{refl\ 1}(s) = E_i(s)\,\rho_L(s) = \frac{-\left(s - \frac{1}{Z_o C_T}\right)}{s^2\left(s + \frac{1}{Z_o C_T}\right)}\ m\left(1 - e^{-T_1 s}\right) . \tag{74}$$

The second reflected voltage waveform at the load occurs a time $2T_D$ later and can be written as:

$$E_{refl\ 2}(s) = E_{refl\ 1}(s)\,\rho_S\,\rho_L(s) = \frac{\left(s - \frac{1}{Z_o C_T}\right)^2 \rho_S}{s^2\left(s + \frac{1}{Z_o C_T}\right)^2}\ m\left(1 - e^{-T_1 s}\right) , \tag{75}$$

where:

$$\rho_S = \frac{R_o + R_S - Z_o}{R_o + R_S + Z_o} . \tag{76}$$

The third reflected voltage waveform at the load is:

$$E_{refl\ 3}(s) = E_{refl\ 1}(s)\,\rho_S{}^2\,\rho_L{}^2(s) = \frac{-\left(s - \frac{1}{Z_o C_T}\right)^3 \rho_S{}^2\, m\left(1 - e^{-T_1 s}\right)}{s^2\left(s + \frac{1}{Z_o C_T}\right)^3} . \tag{77}$$

So the n^{th} reflected voltage waveform at the load is:

$$E_{refl\,(n)}(s) = E_{refl\,1}\,\rho_S^{n-1}\,\rho_L^{n-1}(s)$$

$$= \frac{(-1)^n \left(s - \frac{1}{Z_o C_T}\right)^n \rho_S^{n-1}\, m \left(1 - e^{-T_1 s}\right)}{s^2 \left(s + \frac{1}{Z_o C_T}\right)^n} \quad . \tag{78}$$

The output voltage at the end of the line can be derived by using equations 73 through 78. The output voltage, E_{o1}, due to the input voltage waveform and the first reflection is:

$$E_{o1}(s) = E_i(s) + E_{refl\,1}(s) = E_i(s)\left(1 + \rho_L(s)\right)$$

$$= \frac{\frac{2m}{Z_o C_T}\left(1 - e^{-T_1 s}\right)}{s^2 \left(s + \frac{1}{Z_o C_T}\right)} \quad , \tag{79}$$

It should be noted that equations 79 and 46 are equal (though they were derived differently), when $R = Z_o$. At first glance it may appear that equation 79 is twice the value of equation 46, but the apparent discrepancy is resolved by noting that m has been defined differently for each equation.

The output voltage, E_{o2}, due to the first reflected voltage waveform returning from the driving source will be:

$$E_{o2}(s) = \rho_S E_{refl\,1}(s) + E_{refl\,2}(s) = E_i(s)\,\rho_S\,\rho_L(s)\left(1 + \rho_L(s)\right)$$

$$= \frac{\frac{-2m}{Z_o C_T}\rho_S \left(s - \frac{1}{Z_o C_T}\right)\left(1 - e^{-T_1 s}\right)}{s^2 \left(s + \frac{1}{Z_o C_T}\right)^2} \cdot U(t - 2T_D) \quad . \tag{80}$$

Similarly, the output voltage, E_{o3}, due to the second reflected voltage waveform returning from the driving source is:

$$E_{o3}(s) = E_i(s)\,\rho_S^2\,\rho_L^2(s)\left(1 + \rho_L(s)\right),$$

or:

$$E_{o3}(s) = \frac{\frac{2m}{Z_o C_T}\rho_S^2 \left(s - \frac{1}{Z_o C_T}\right)^2 \left(1 - e^{-T_1 s}\right)}{s^2 \left(s + \frac{1}{Z_o C_T}\right)^3} \cdot U\left(t - 4T_D\right) \quad . \qquad (81)$$

Finally, the n^{th} output voltage waveform will be:

$$E_{on}(s) = E_i(s)\,\rho_S^{n-1}\,\rho_L^{n-1}(s)\left(1 + \rho_L(s)\right)$$

$$= \frac{(-1)^{n-1}\left(\frac{2m}{Z_o C_T}\right)\rho_S^{n-1}\left(s - \frac{1}{Z_o C_T}\right)^{n-1}\left(1 - e^{-T_1 s}\right)}{s^2\left(s + \frac{1}{Z_o C_T}\right)^n} \cdot$$

$$U\left(t - 2(n-1)\,T_D\right); \qquad (82)$$

therefore, the general equation for the output voltage at the end of the line (point C in Figure 7-27) can be formulated as a summation of the individual reflected voltage components:

$$E_{out}(s) = E_{o1}(s) + E_{o2}(s) + E_{o3}(s) + \ldots + E_{on}(s) + \ldots$$

$$= \sum_{n=1}^{\infty} \left[\frac{(-1)^{n-1}\left(\frac{2m}{Z_o C_T}\right)\rho_S^{n-1}\left(s - \frac{1}{Z_o C_T}\right)^{n-1}\left(1 - e^{-T_1 s}\right)}{s^2\left(s + \frac{1}{Z_o C_T}\right)^n} \cdot \right.$$

$$\left. U\left(t - 2(n-1)\,T_D\right) \right] . \qquad (83)$$

The inverse LaPlace transforms for equations 79, 80, and 81 can be found in standard tables. The inverses can be written to take into account the time delays the following way.

The inverse LaPlace transform of equation 79 is:

$$e_{o1}(t) = \mathcal{L}^{-1}\left[\frac{\frac{2m}{Z_oC_T}\left(1 - e^{-T_1 s}\right)}{s^2\left(s + \frac{1}{Z_oC_T}\right)}\right]$$

$$= 2mZ_oC_T\left(\frac{-t}{e^{Z_oC_T}} + \frac{t}{Z_oC_T} - 1\right) \cdot U(t)$$

$$- 2mZ_oC_T\left(e^{\frac{-(t - T_1)}{Z_oC_T}} + \frac{t - T_1}{Z_oC_T} - 1\right) \cdot U(t - T_1). \qquad (84)$$

Likewise, the inverse transform of equation 80 becomes:

$$e_{o2}(t) = 2m\rho_S Z_oC_T\left[\left(-3 + \frac{t - 2T_D}{Z_oC_T}\right) + \left(3 + \frac{2(t - 2T_D)}{Z_oC_T}\right)\cdot\right.$$

$$\left.e^{-\left(\frac{t - 2T_D}{Z_oC_T}\right)}\right] \cdot U(t - 2T_D) - 2m\rho_S Z_oC_T \cdot$$

$$\left[\left(-3 + \frac{t - 2T_D - T_1}{Z_oC_T}\right) + \left(3 + \frac{2(t - 2T_D - T_1)}{Z_oC_T}\right)\cdot\right.$$

$$\left.e^{-\left(\frac{t - 2T_D - T_1}{Z_oC_T}\right)}\right] \cdot U(t - 2T_D - T_1) \ . \qquad (85)$$

Finally, the inverse transform of equation 81 produces:

$$e_{o3}(t) = 2m\rho_S{}^2 Z_o C_T \left[-5 + \frac{t - 4T_D}{Z_o C_T} + \left(5 + \frac{4(t - 4T_D)}{Z_o C_T} + \frac{2(t - 4T_D)^2}{(Z_o C_T)^2} \right) \cdot e^{\frac{-(t - 4T_D)}{Z_o C_T}} \right] \cdot U(t - 4T_D) -$$

$$2m\rho_S{}^2 Z_o C_T \left[-5 + \frac{t - 4T_D - T_1}{Z_o C_T} + \left(5 + \frac{4(t - 4T_D - T_1)}{Z_o C_T} + \frac{2(t - 4T_D - T_1)^2}{(Z_o C_T)^2} \right) \cdot e^{\frac{-(t - 4T_D - T_1)}{Z_o C_T}} \right] \cdot U(t - 4T_D - T_1) \quad . \quad (86)$$

A general form equation can be established for $e_{o\,(n)}(t)$ as an extension of the preceeding equations. Such a general equation can then be used to obtain a general relationship for $e_{out}(t)$ derived from equation 83.

However, for our purposes, the output voltage needs to be defined only for a period of time long enough to determine the maximum amount of overshoot and undershoot. The following can be written for the first three reflections (a sufficient time interval):

$$e_{out}(t) = \sum_{n=1}^{3} \left\{ 2m\rho_S{}^{n-1} Z_o C_T \left[\left(\frac{t - 2T_D(n-1)}{Z_o C_T} - (2n-1) \right) \cdot \left(1 - e^{\frac{t - 2T_D(n-1)}{Z_o C_T}} \right) + \left((n-1) e^{\frac{-\left(t - 2T_D(n-1)\right)}{Z_o C_T}} \right) \cdot \left(\frac{2\left(t - 2T_D(n-1)\right)}{Z_o C_T} + (n-2)\left(\frac{t - 2T_D(n-1)}{Z_o C_T} \right)^2 \right) \right] \cdot U\left(t - 2(n-1)T_D\right) \right\}$$

$$-\sum_{n=1}^{3}\left\{2m\rho_S^{n-1}\,Z_oC_T\left[\left(\frac{t-2T_D(n-1)-T_1}{Z_oC_T}-(2n-1)\right)\cdot\left(1-e^{\frac{-\left(t-2T_D(n-1)-T_1\right)}{Z_oC_T}}\right)+\left((n-1)\,e^{\frac{\left(t-2T_D(n-1)-T_1\right)}{Z_oC_T}}\right)\cdot\left(\frac{2\left(t-2T_D(n-1)-T_1\right)}{Z_oC_T}+(n-2)\left(\frac{t-2T_D(n-1)-T_1}{Z_oC_T}\right)^2\right)\right]\cdot U\left(t-2(n-1)T_D-T_1\right)\right\}\,,\quad \text{for } t<6T_D\,, \tag{87}$$

where:

$$m=\frac{Z_oE_1}{(R_o+R_S+Z_o)T_1}\,,$$

$$T_1=1.2\,t_r\,,$$

and t_r is the 10 to 90% rise time of the voltage at point A in Figure 7-27. Figs. 3-13 through 3-15 are generated with a computer program using an extension of equation 87 in which the first 7 reflections were considered.

An extension of equation 87 was used in generating Tables 3-22 and 3-23 and may also be used to determine maximum line length for specified undershoot and overshoot, instead of using equations 12 and 13. This derivation follows.

For $C_T = 0$ and $t < 6T_D$, equation 87 reduces to:

$$e_{out}(t)=2\,mt\,U(t)-2m\,(t-T_1)\,U\,(t-T_1)+2m\rho_S\,.\,(t-2T_D)\,U\,(t-2T_D)-2m\rho_S\,(t-2T_D-T_1)\,U\,(t-2T_D-T_1)+2m\rho_S^{\,2}\,(t-4T_D)\,U\,(t-4T_D)-2m\rho_S^{\,2}\,(t-4T_D-T_1)\,.\,U\,(t-4T_D-T_1)\,. \tag{88}$$

This equation can also be derived by starting from equation 5.

Using a lattice diagram, it is found that the maximum overshoot occurs at $t = T_1$. Substituting $t = T_1$ into equation 88 gives:

$$E_{max} = 2m \left[T_1 + \rho_S (T_1 - 2T_D) \right] , \qquad (89)$$

$$\text{for } 2T_D < T_1 < 4T_D ;$$

and:

$$E_{max} = 2mT_1 ,$$

$$\text{for } T_1 \leq 2T_D . \qquad (90)$$

In both cases,

$$m = \frac{Z_o E_1}{(R_o + Z_o + R_s)T_1} ,$$

$$T_1 = 1.2t_r ,$$

$$T_D = t_{pd} \cdot \ell ,$$

and

t_{pd} = line delay in nanoseconds/inch,

ℓ = line length in inches.

By definition,

$$E_{max} = E_1 \frac{(100 + O.S.)}{100} , \qquad (91)$$

where E_1 is the voltage change at the output of the driving gate, and O.S. is the percent overshoot based on logic swing level. Thus by substituting into equation 89, the percent overshoot can be obtained:

$$\%O.S. = \left[-1 + \frac{2 Z_o}{Z_o + R_S + R_o} \quad (1 + \rho_S) - \frac{4\rho_S t_{pd} \ell Z_o}{1.2\, t_r (Z_o + R_S + R_o)} \right] \cdot 100 \ , \tag{92}$$

$$\text{for } 2t_{pd} < T_1 < 4t_{pd} \ .$$

Equation 92 gives the overshoot (as a percentage of the logic swing) that occurs for a particular length of line, assuming zero capacitance at the end of the line. If the two way propagation delay of the line is equal to or greater than T_1, then this particular length of line is:

$$\ell \geq \frac{1.2\, t_r}{2t_{pd}} \ . \tag{93}$$

If equation 93 is satisfied, then the overshoot reaches a maximum value which can be solved for by using equation 90:

$$\%O.S._{max} = 100 \left(\frac{2 Z_o}{Z_o + R_S + R_o} - 1 \right) \ . \tag{94}$$

If the length of line is less than that specified in equation 93, the line length can be found from equation 92, given the permissible overshoot for a given design:

$$\ell = \left[\frac{2 Z_o}{R_o + Z_o + R_S} \cdot (1 + \rho_S) - \frac{(100 + O.S.)}{100} \right] \cdot \left(\frac{(R_o + Z_o + R_S)\, 1.2\, t_r}{4 Z_o \rho_S\, t_{pd}} \right) \ . \tag{95}$$

In this relation , it is necessary that:

$$\ell < \frac{1.2\, t_r}{2t_{pd}} \ .$$

The maximum permissible line length with capacitance loading can be approximated in a manner similar to that used to establish a maximum open line length in a previous section:

$$\frac{\ell}{\ell_{max}} = \frac{t_{pd}\sqrt{1 + \dfrac{C_T}{C_o \ell_{max}}}}{t_{pd}} \quad . \tag{96}$$

Solving for ℓ_{max}:

$$\ell_{max} = \frac{-\dfrac{C_T}{C_o} + \sqrt{\left(\dfrac{C_T}{C_o}\right)^2 + 4\ell^2}}{2} \quad , \tag{97}$$

where C_T is the total lumped capacitance in pF, C_o is the intrinsic line capacitance in pF/in, and ℓ is the length of line in inches defined in equation 95.

Using a lattice diagram, it has been found that the maximum undershoot occurs when $t = 2T_D + T_1$. Substituting this information into equation 88 produces the relation:

$$E_{min} = 2m\left((2T_D + T_1) - 2T_D + \rho_S T_1 + \rho_S{}^2 (T_1 - 2T_D)\right) \quad , \tag{98}$$

for:

$$2T_D < T_1 < 4T_D \quad ,$$

$$E_{min} = 2m\,(1 + \rho_S)\,T_1 \quad , \tag{99}$$

$$T_1 \leq 2t_{pd} \quad .$$

By definition,

$$E_{min} = E_1 \frac{(100 - U.S.)}{100} \quad , \tag{100}$$

where U.S. is the percent undershoot. Equation 98 can be used to form a useful

relationship, which expresses the undershoot in terms of circuit parameters:

$$\%U.S. = \left(1 - \frac{2Z_o}{Z_o + R_S + R_o}\left(1 + \rho_S + \rho_S{}^2\right) + \frac{4\rho_S{}^2 t_{pd} \ell Z_o}{1.2\, t_r (Z_o + R_S + R_o)}\right) \cdot 100 \qquad (101)$$

for:

$$2T_D < T_1 < 4T_D$$

and:

$$\ell < \frac{1.2\, t_r}{2\, t_{pd}} .$$

Thus equation 101 gives the undershoot as a percentage of the logic swing – for a particular length of line.

If equation 93 is satisfied, then the undershoot reaches a maximum value which can be found from equation 99 to be:

$$\%U.S._{max} = 100\left(1 - \frac{2\,Z_o}{Z_o + R_S + R_o} \cdot (1 + \rho_S)\right) . \qquad (102)$$

On the other hand, if the length of line is less than specified in equation 93, the line length can be found from equation 101 once the permissible undershoot has been specified. Solving:

$$\ell = \left(\frac{2\,Z_o}{Z_o + R_S + R_o}(1 + \rho_S + \rho_S{}^2) - \frac{(100 - U.S.)}{100}\right) \cdot \frac{(Z_o + R_S + R_o)\ 1.2\, t_r}{4\, Z_o \rho_S{}^2 t_{pd}} , \qquad (103)$$

for:

$$\ell < \frac{1.2\, t_r}{2t_{pd}} .$$

Equations 95 and 97 can be used to find the maximum open line length (instead of equations 12 and 13) when the maximum percentage overshoot has been specified. Equations 97 and 103 can be used when the maximum undershoot is specified. Of course, a more exact value for the maximum permissible line length is found when a computer program is used to generate the values using an extension of equation 87. This was done to generate Figures 3-13, 3-14, and 3-15. The first seven reflections (n = 7) were used to accurately define the open line length required to limit overshoot and undershoot for a wide range of load capacitances. Equations 94 and 102 were used to generate the values given in Figures 3-22 and 3-23 using a computer program.

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CHAPTER 8 MECL Applications

This chapter presents design ideas for using MECL circuits. The majority of circuits shown here use MECL II parts, as this family was introduced before the MECL III and MECL 10,000 families. However most of the MECL II circuits may be built with MECL 10,000 or MECL III parts, giving a corresponding increase in speed. Conversely, the MECL III designs can use MECL II or MECL 10,000 devices to save power, when the speed is not required.

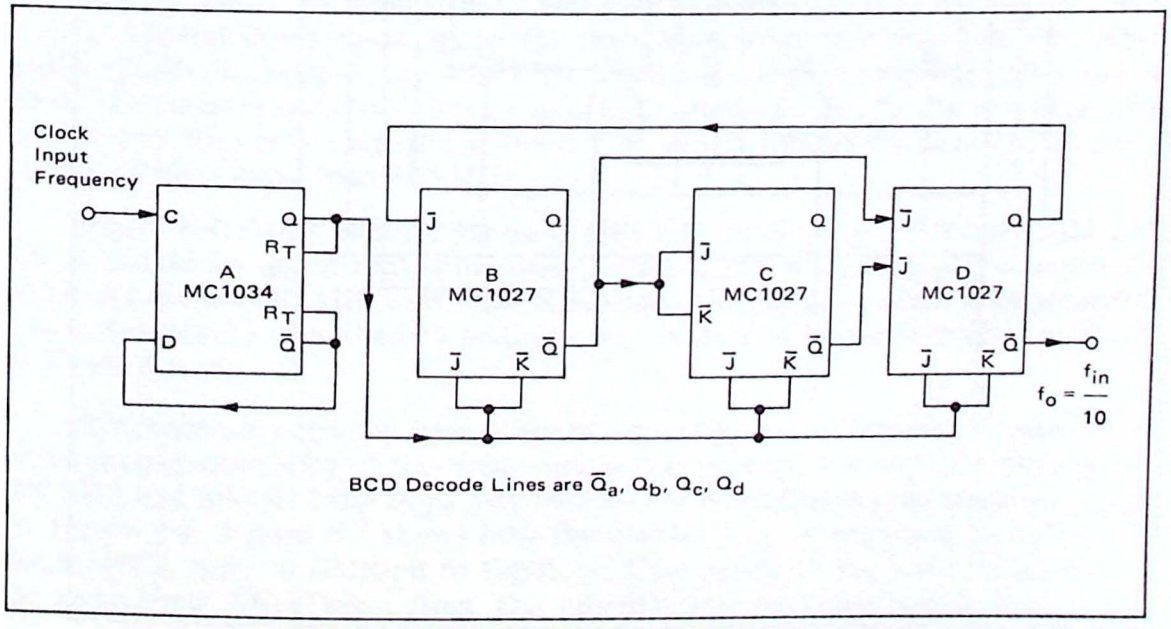
Some of the MECL III circuits do not show pulldown resistors. These circuits are intended only to illustrate the logic connections and either pulldown resistors or line termination resistors must be incorporated in these designs.

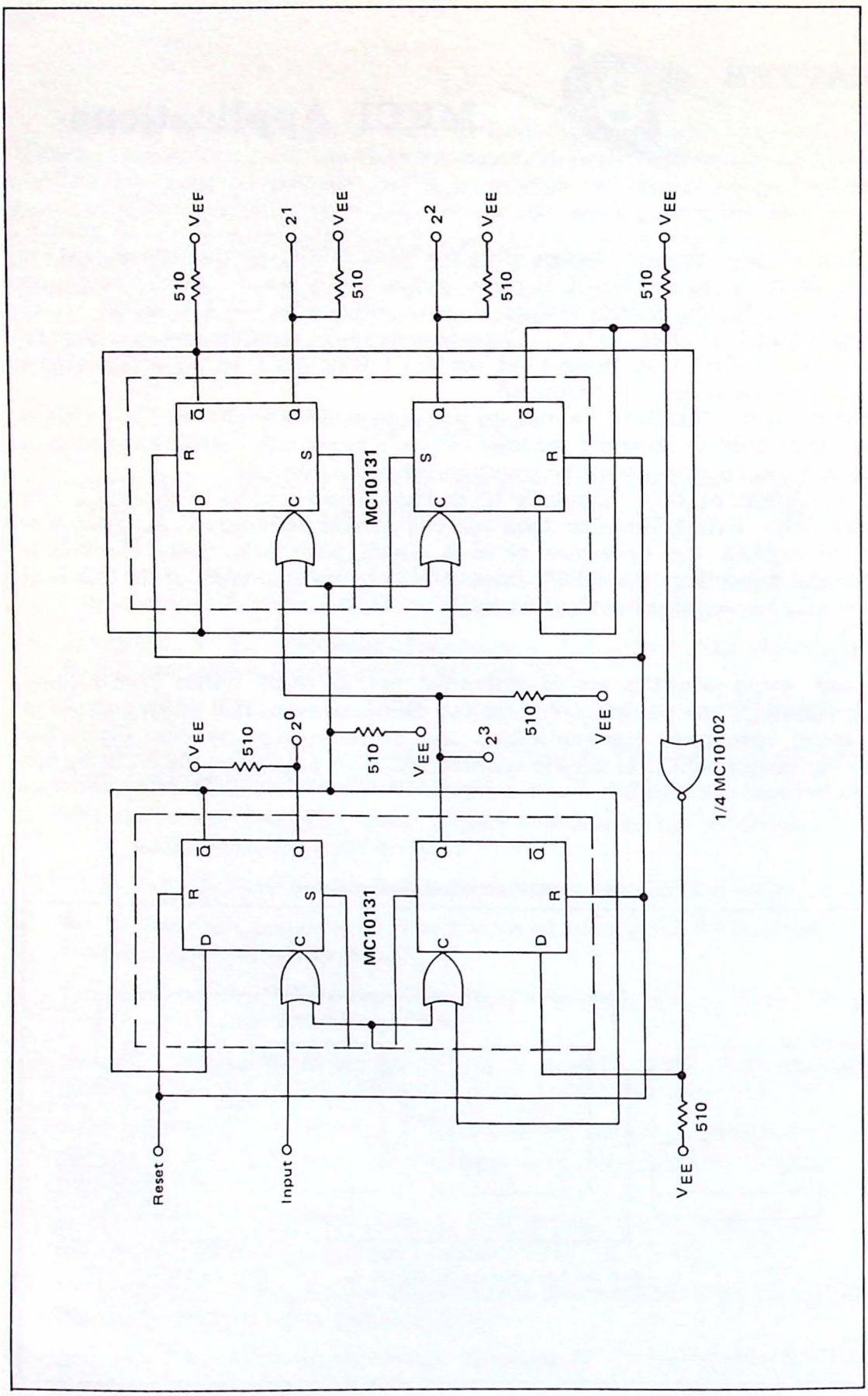
The intent of this chapter is to present various circuits to the MECL user together with a description of their use and general performance. No attempt is made to explain the operation of each circuit completely. Since Motorola is continually expanding the MECL lines, it is expected that some of the following circuits may be simplified by future complex functions.

Counters

High speed counters are an important part of many system designs. Since MECL flip-flops are the industry's fastest, MECL counters find widespread use in high speed computer, communication and instrumentation systems. Figure 8-1 shows the fastest MECL II decade counter. MC1027s are used in the divide-by five section because the multiple $\overline{J}$ and $\overline{K}$ inputs allow use of the BCD code without an

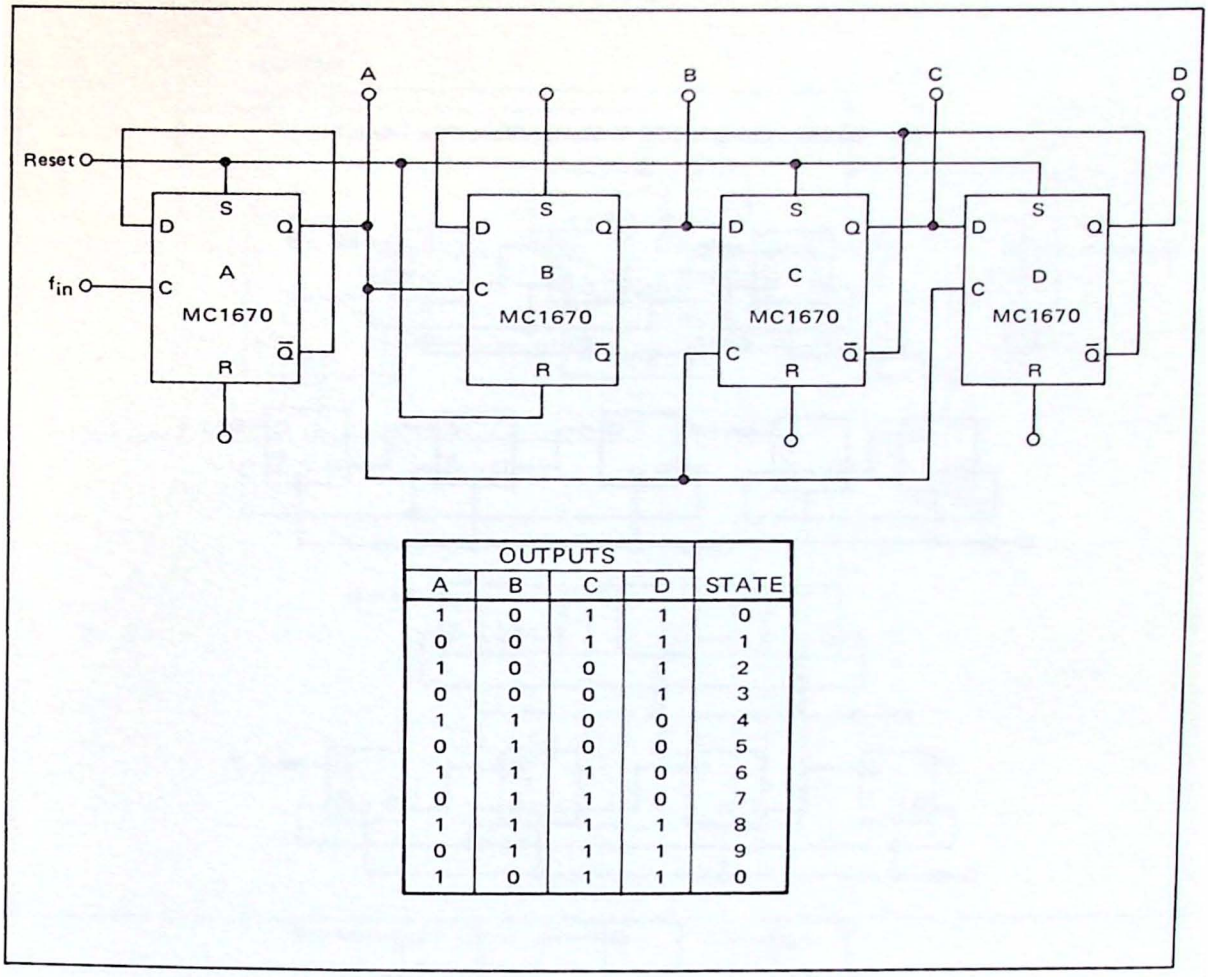
8-1: 100 MHz MECL II Decade Counter





8-2: BCD MECL 10,000 Decade Counter

8-3: 300 MHz MECL III Decade Counter
(No Additional Gates Required)



OUTPUTS				
A	B	C	D	STATE
1	0	1	1	0
0	0	1	1	1
1	0	0	1	2
0	0	0	1	3
1	1	0	0	4
0	1	0	0	5
1	1	1	0	6
0	1	1	0	7
1	1	1	1	8
0	1	1	1	9
1	0	1	1	0

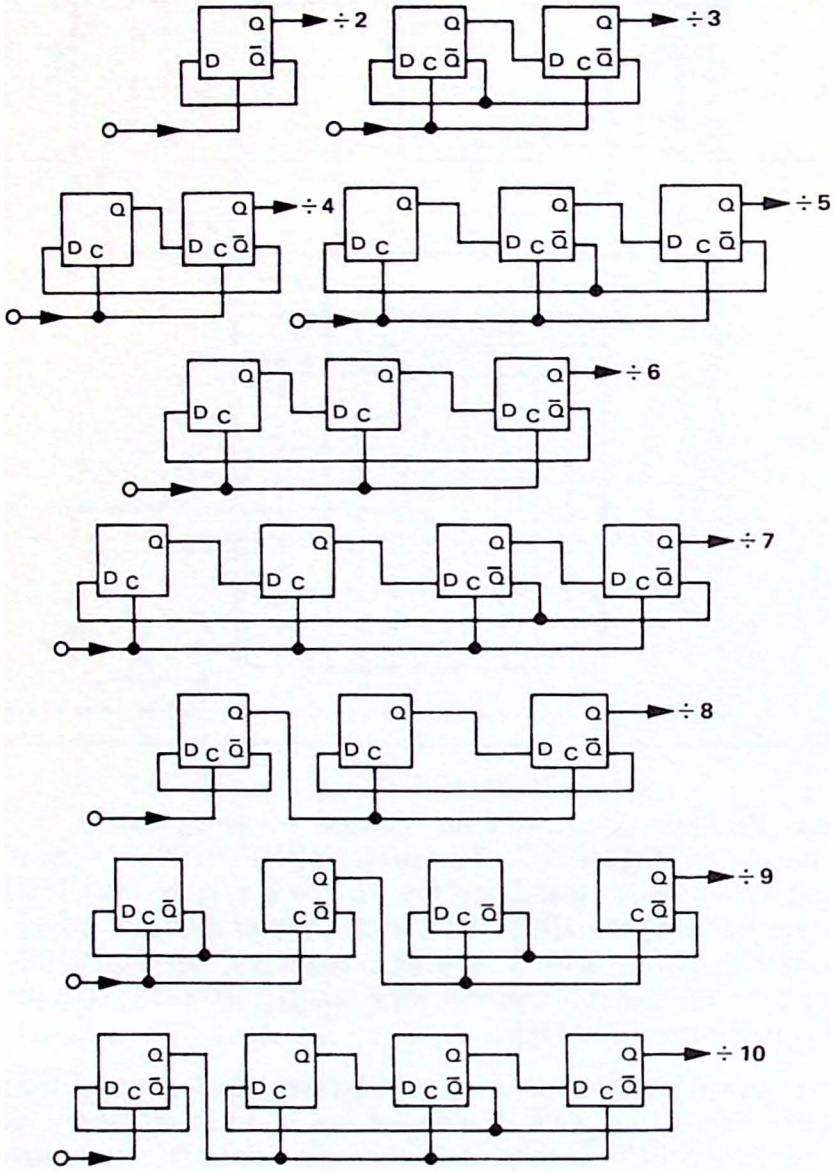
additional gate. Package count can be reduced by going to the MC10131 dual flip-flops as shown in Figure 8-2. The gate (1/4-MC10102) is required for BCD coding. Typical input clock speed for this circuit is greater than 150 MHz. When higher speeds are needed, the MECL III decade counter shown in Figure 8-3 may be used. The counter does not operate in a BCD sequence, but the 60/40% duty cycle output may be a better signal if a slower logic family follows the counter. The speed of this circuit is more than 300 MHz.

Figure 8-4 shows circuits for using MECL D flip-flops to count from 2 through 10. It should be noted that some counts are not in a natural binary sequence and some circuits use the MECL Wired-OR feature. The divide-by-seven arrangement of Figure 8-4 may be simplified by adding a gate in place of the extra flip-flop as shown in Figure 8-5.

Synchronous counters have a speed advantage when decoding is required or when propagation delay of the total counter is important. The multiple inputs of the MC1013 and MC1027 flip-flops may be used for synchronous counting as illustrated in Figure 8-6. Figure 8-7 shows how the counter may be expanded to 8 stages by using MECL gates in addition to flip-flops. Gate delays to the $\overline{J}$ and $\overline{K}$ inputs must be considered when computing the circuit's top operating speed. Even longer

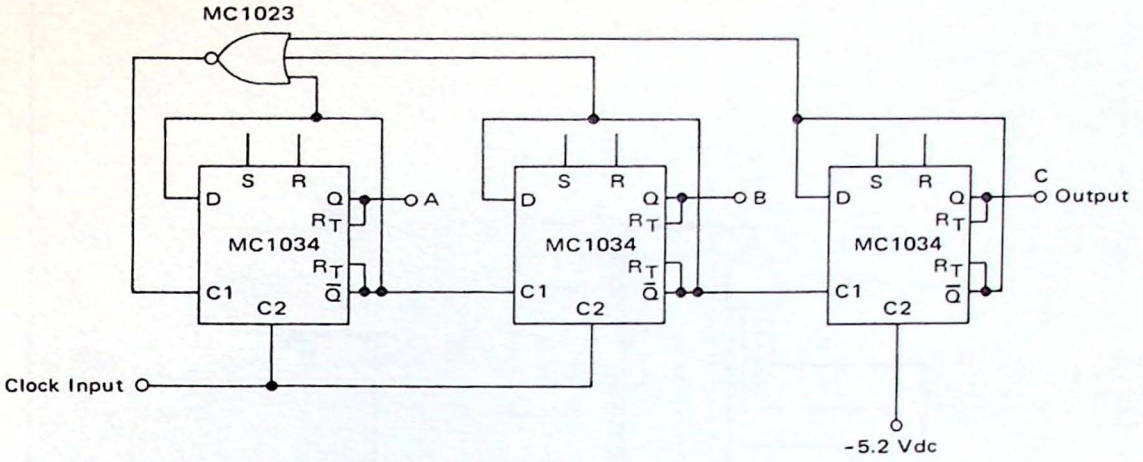
(Continued on Page 174)

8-4: Dividers Using MECL D Master-Slave Flip-Flops



NOTE: Pulldown Resistors Not Shown

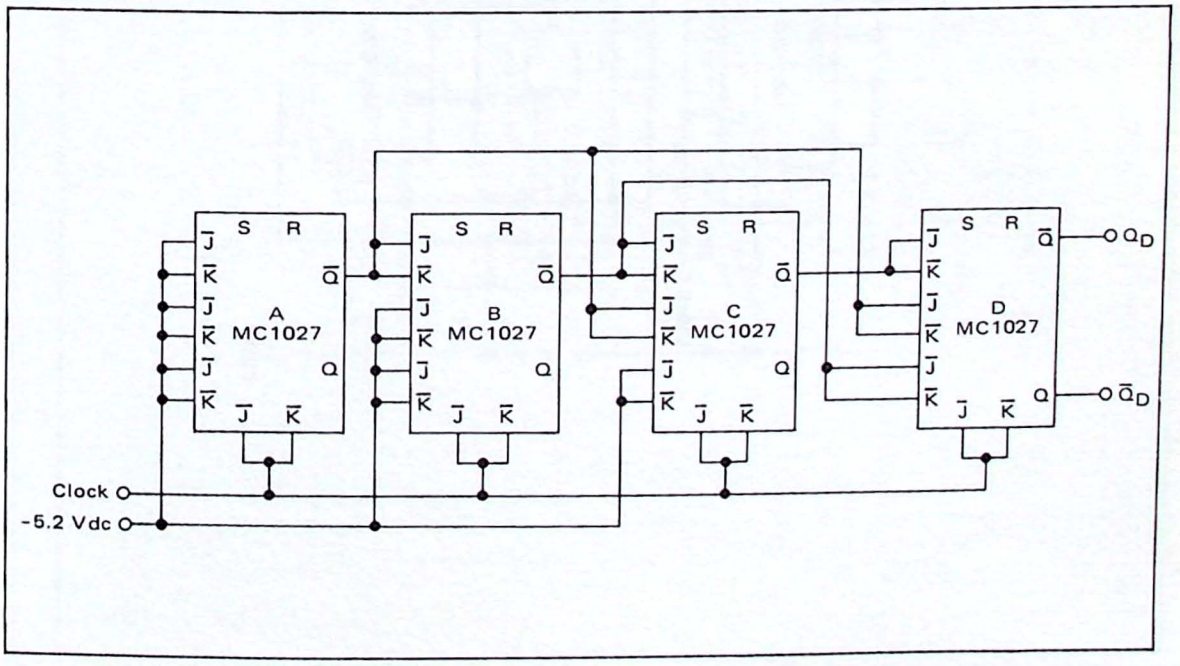
8-5: High Speed Divide-By-Seven Counter

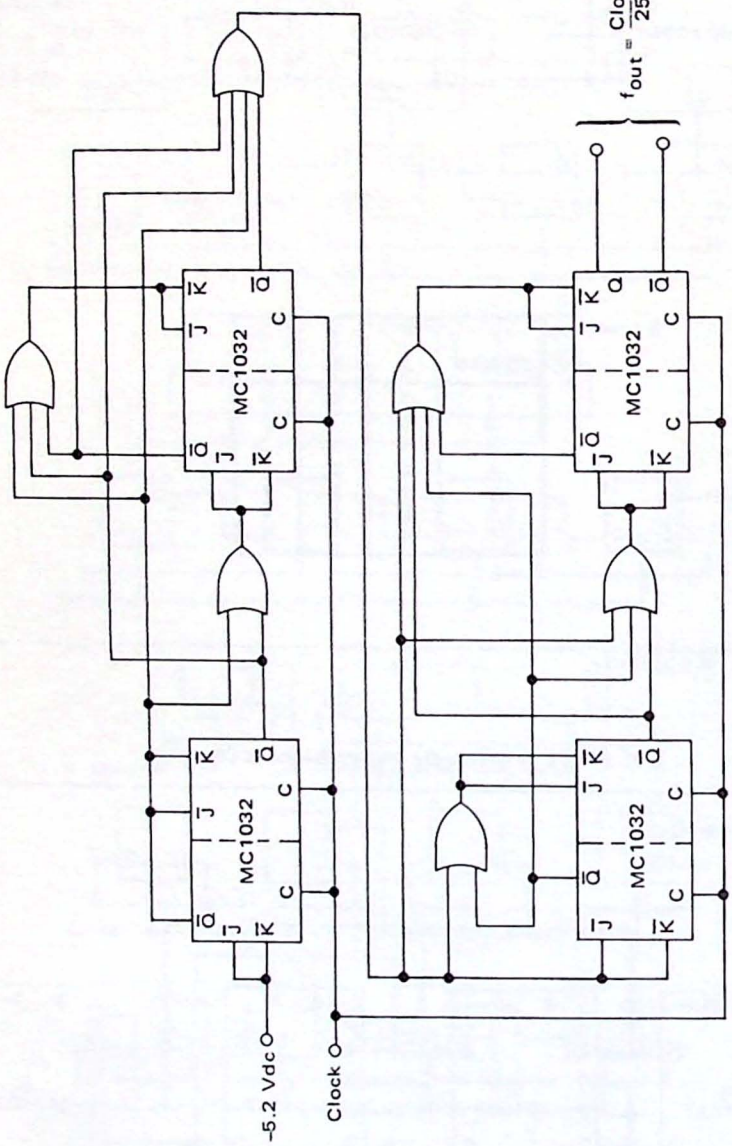


STATE	1 A	2 B	4 C
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

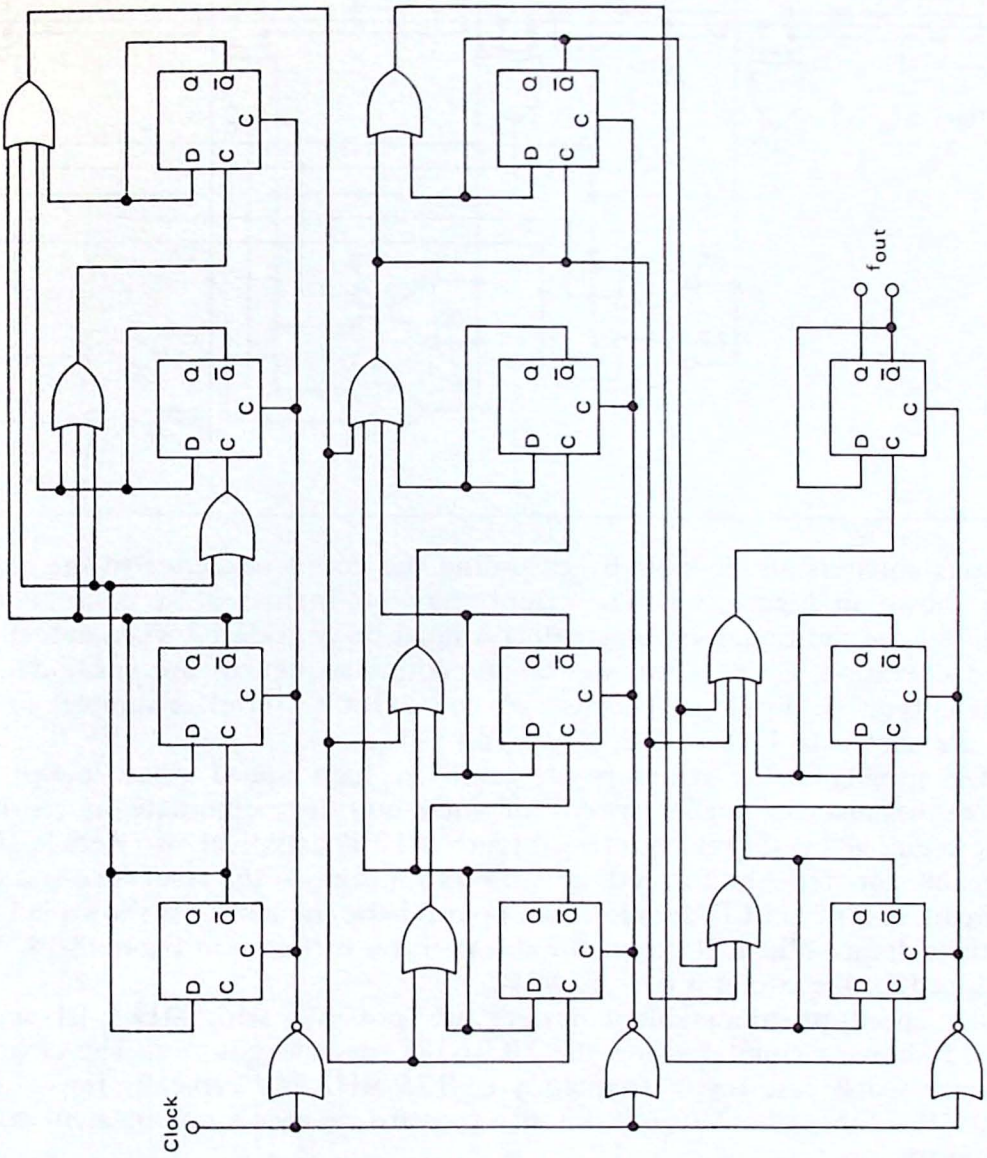
0→1

8-6: MECL II Divide-By-16 Synchronous Counter



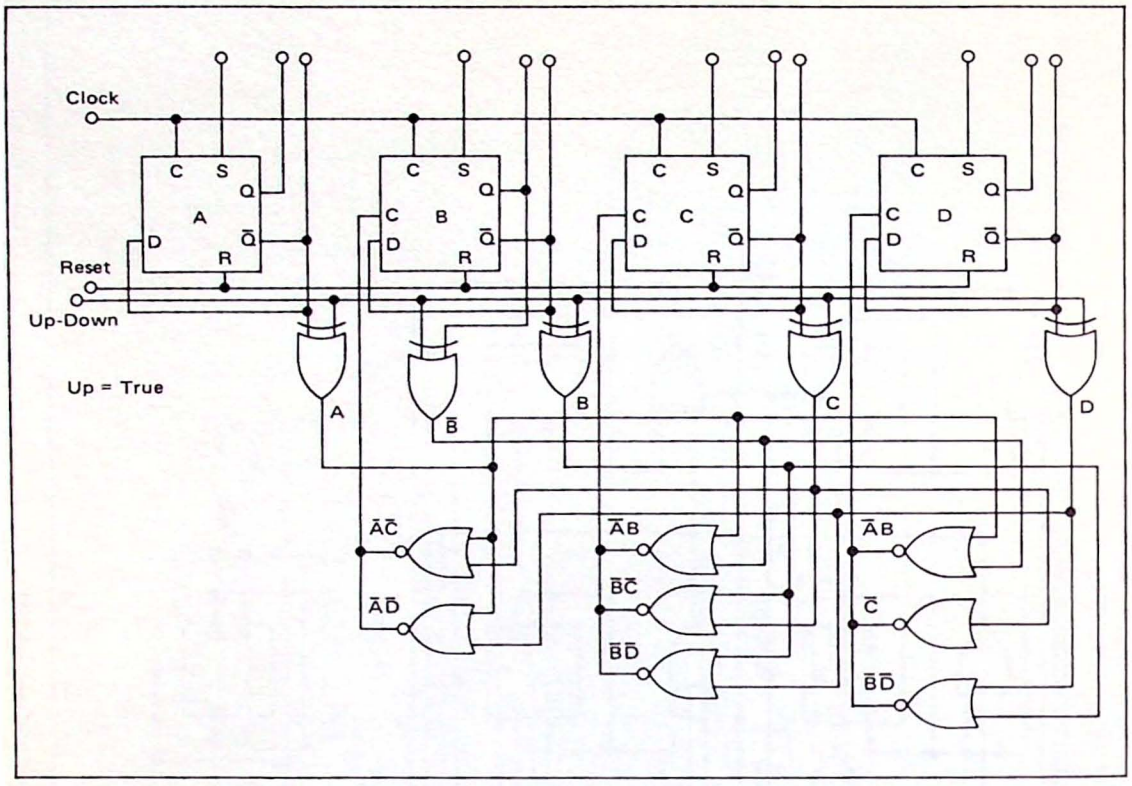


8-7: MECL II Divide-By-256 Synchronous Counter



8-8: 11 Stage MECL III Synchronous Counter

8-9: MECL Synchronous Excess Three Up-Down Counter



synchronous counters are possible by cascading the count sequence to the other C input, as shown in Figure 8-8. The count may be increased by continuing the sequence, but the additional series-gate delays must be considered when determining top speed operation. Circuits for non-binary count sequences are easily designed with MECL type D flip-flops, because of the extra C input. Examples of such counters are shown in Figures 8-9, 8-10, and 8-11.

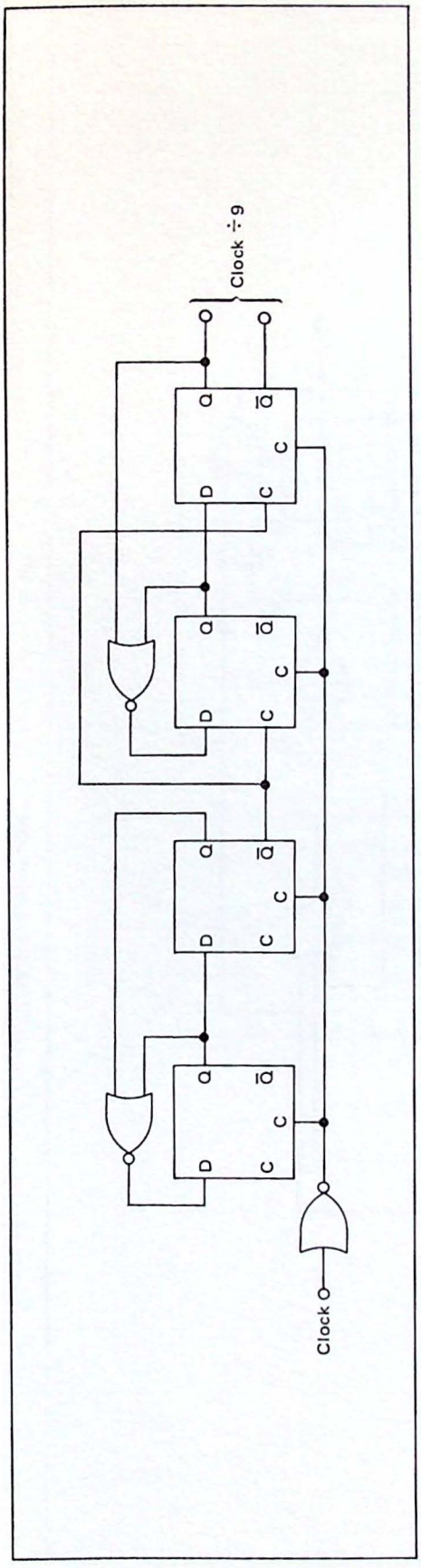
MECL programmable counters are used in high speed phase-locked loop applications because the higher speeds of such counters eliminate much of the prescaling required by slower counters. Figure 8-12 is a typical two decade MECL programmable counter. Early decoding is used to minimize the reset time and speed up the circuit. A typical BCD decade down counter for the circuit is shown in Figure 8-13. A three decade MECL II programmable counter is shown in Figure 8-14. Worst case top speed for the circuit is over 50 MHz.

Higher speed programmable counters are possible with MECL III circuits. Figure 8-15 shows a counter using the MC1678L decade counter. The circuit, as shown, has a worst case toggle frequency of 125 MHz and typically runs at more than 150 MHz. Since the MC1678 counts forward, a nine's complement code is required on the inputs.

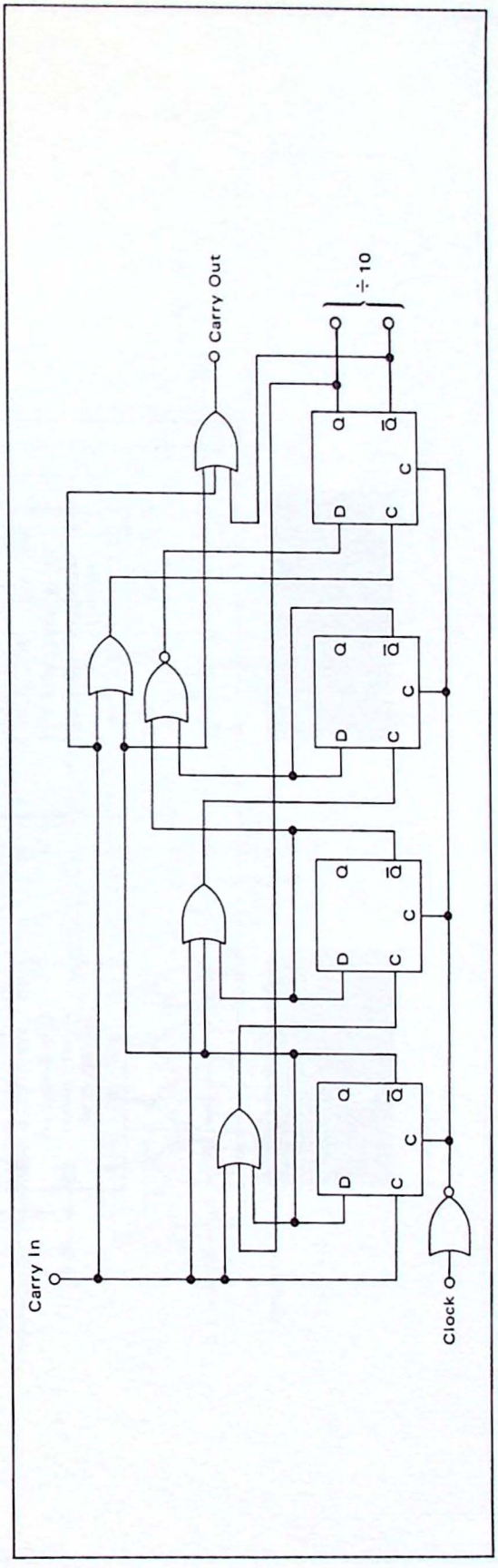
Figures 8-16, 8-17, and 8-18 illustrate typical MECL ring counters. Ring counters are used for ease of decoding and synchronous operation. The counter in Figure 8-18 requires more flip-flops (10), but gives a direct one-of-ten output. These circuits may be of any length needed to give multiphase clocks.

MECL circuit designs with discrete components have been used to obtain even faster performance than with ICs. Figure 8-19 shows a very high speed divide-by-two circuit. Speeds greater than 800 MHz have been achieved using the MMT3960 transistors and over 1 GHz using the MMT8015 transistors.

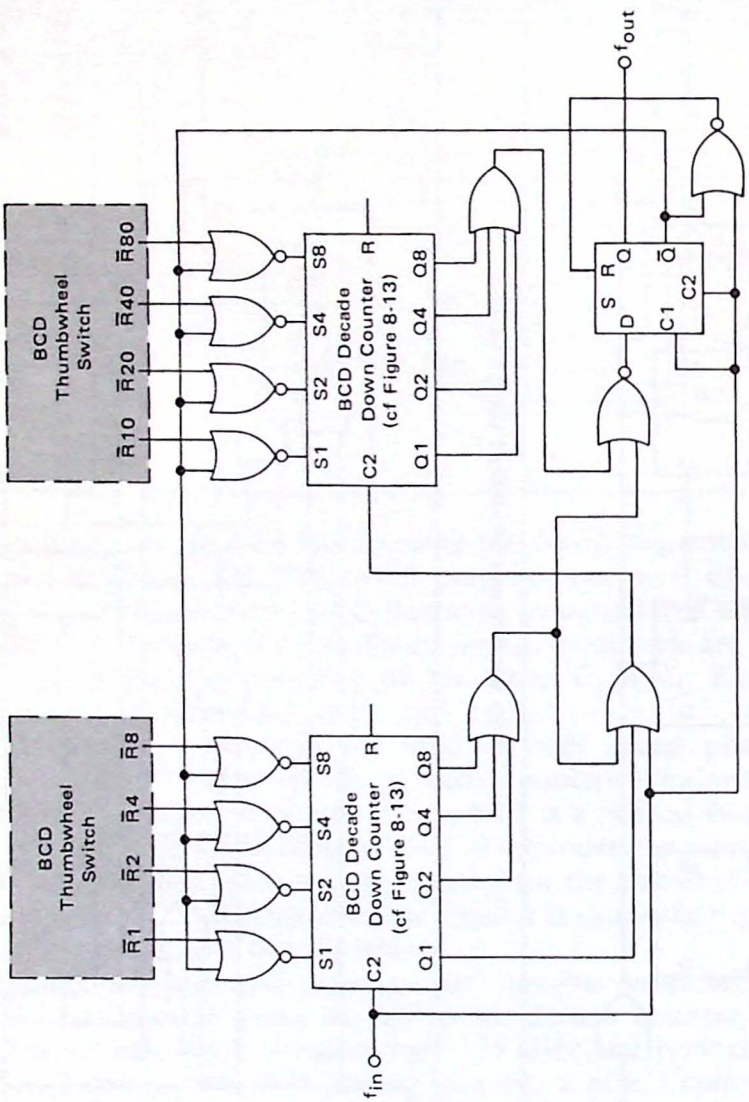
(Continued on Page 182)



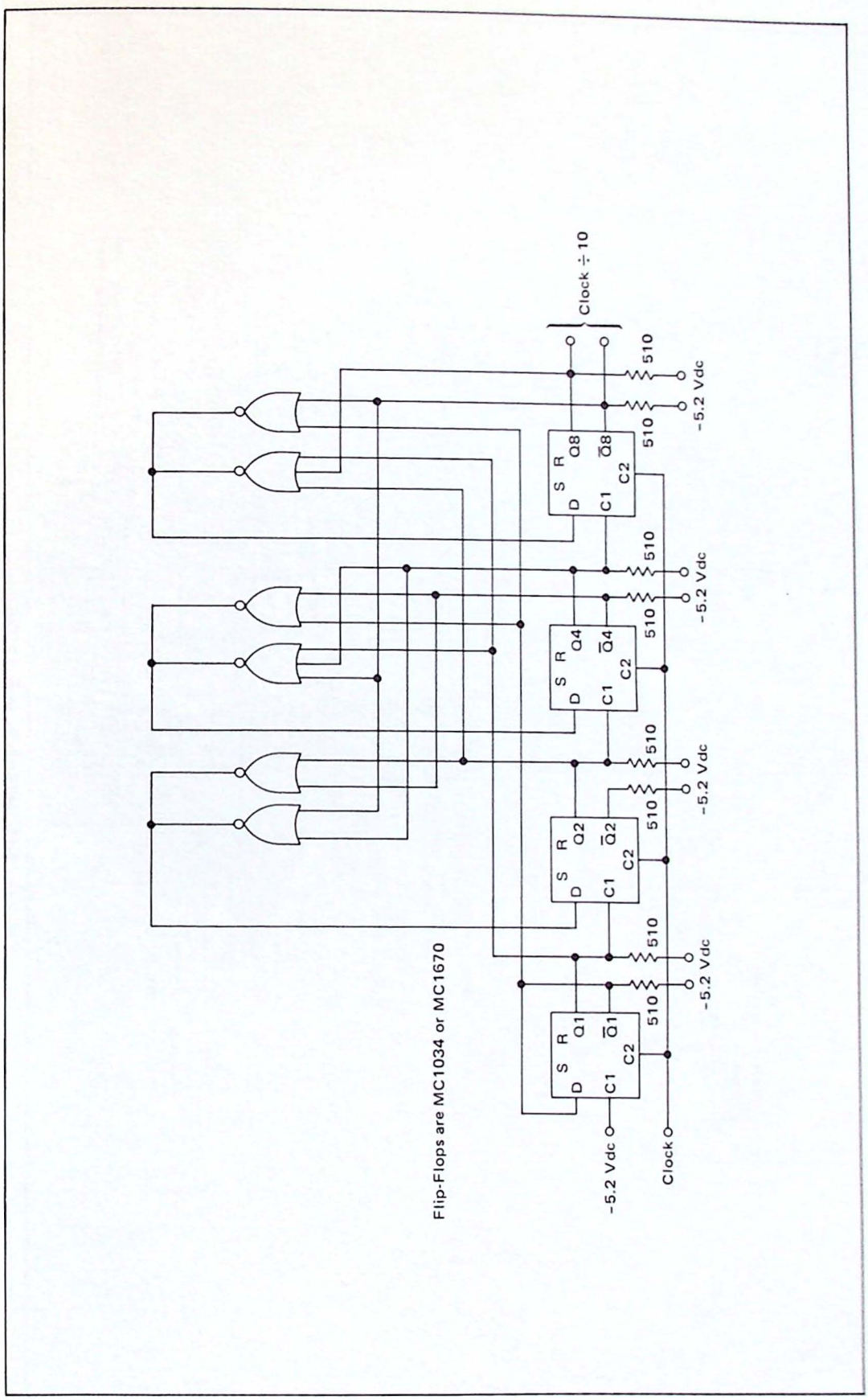
8-10: Synchronous Divide-By-9 (3x3) Counter



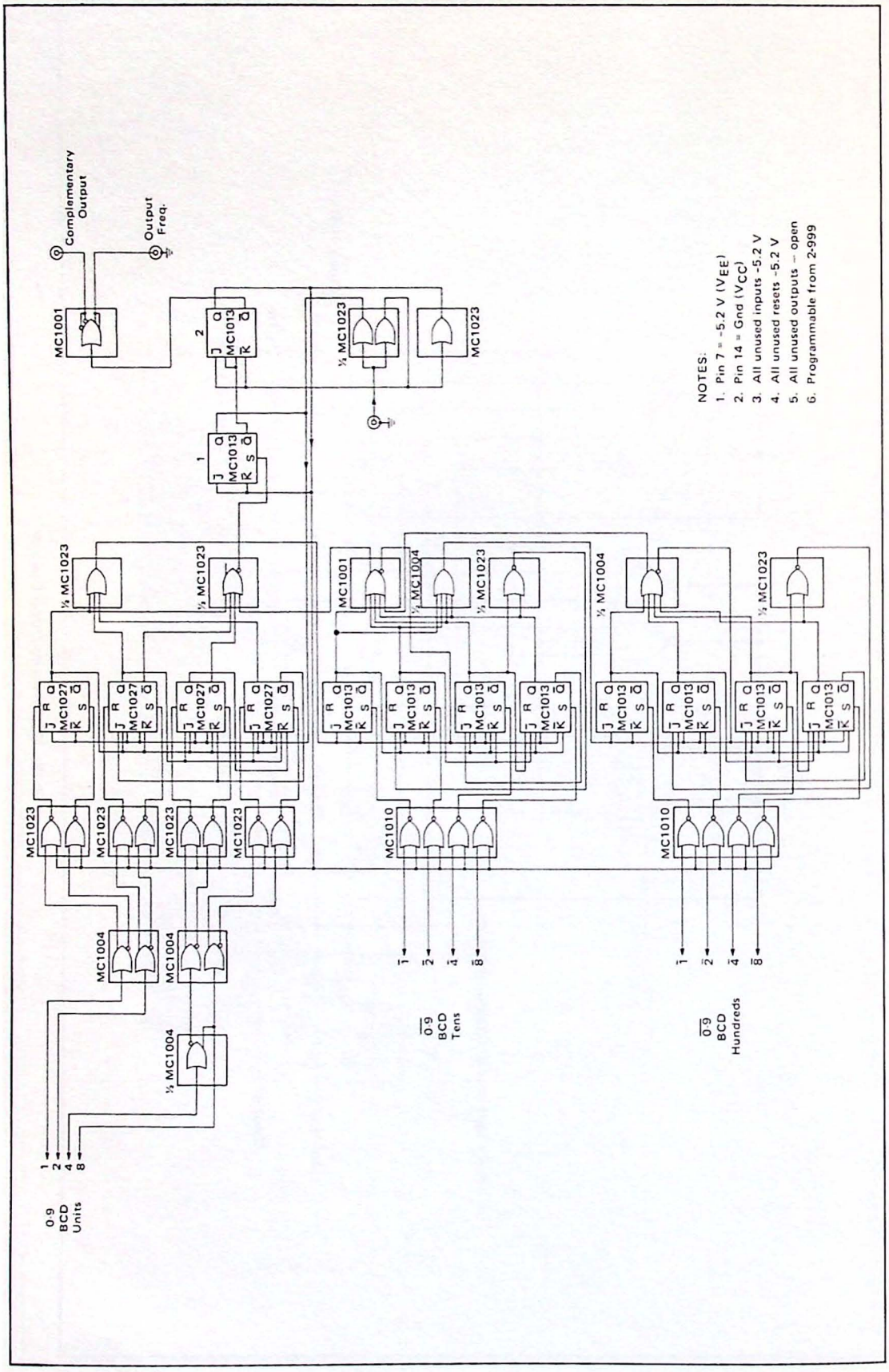
8-11: Synchronous Divide-By-10 Counter



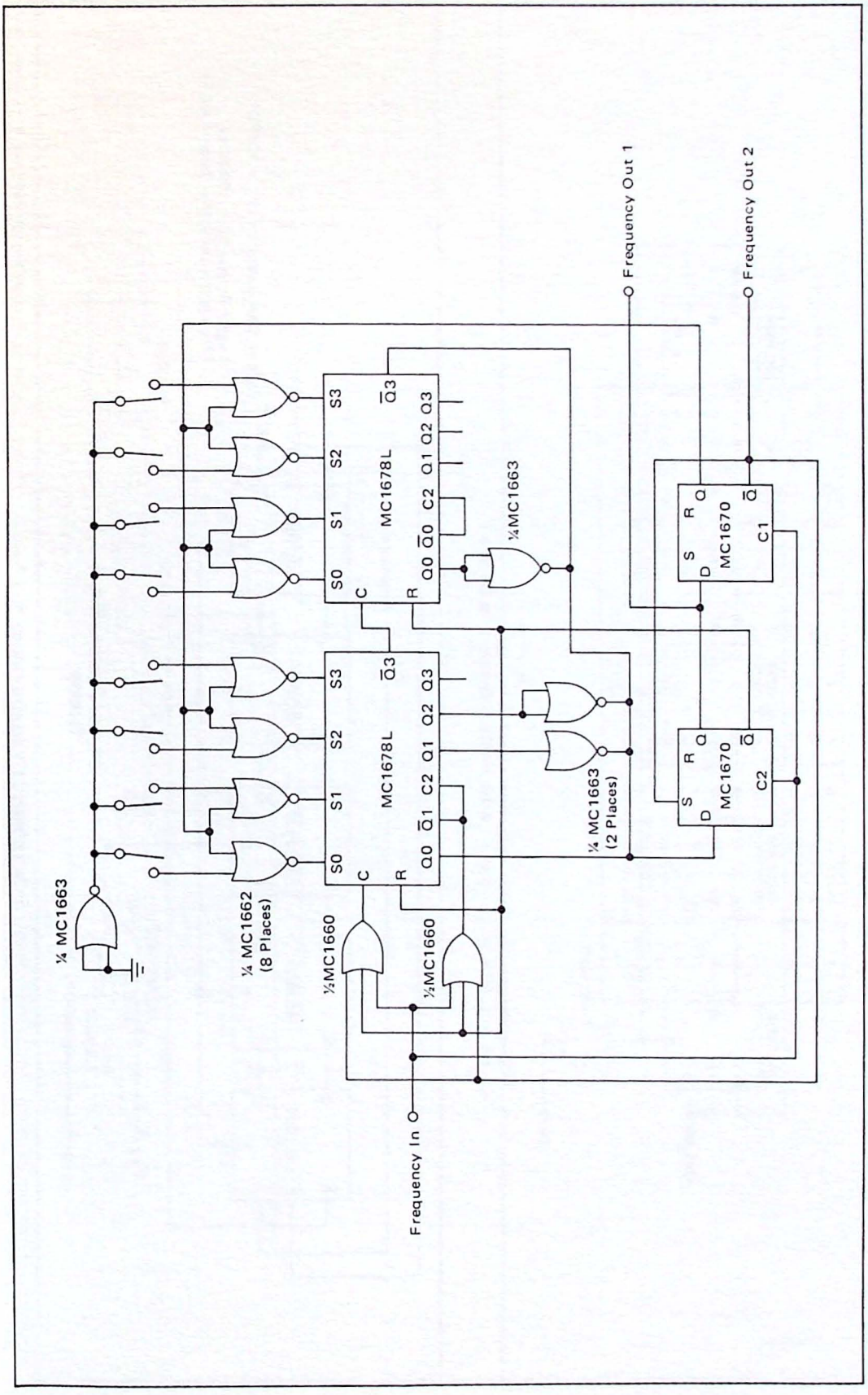
8-12: BCD Programmable Down Counter (N = 1 to 99)



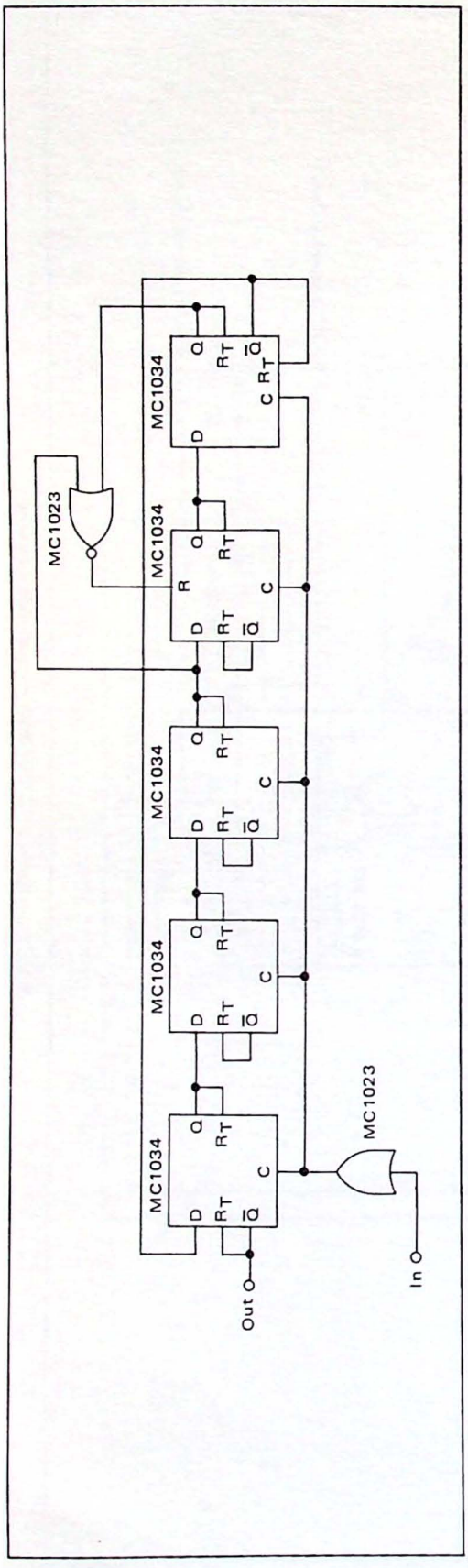
8-13: BCD Decade Down Counter



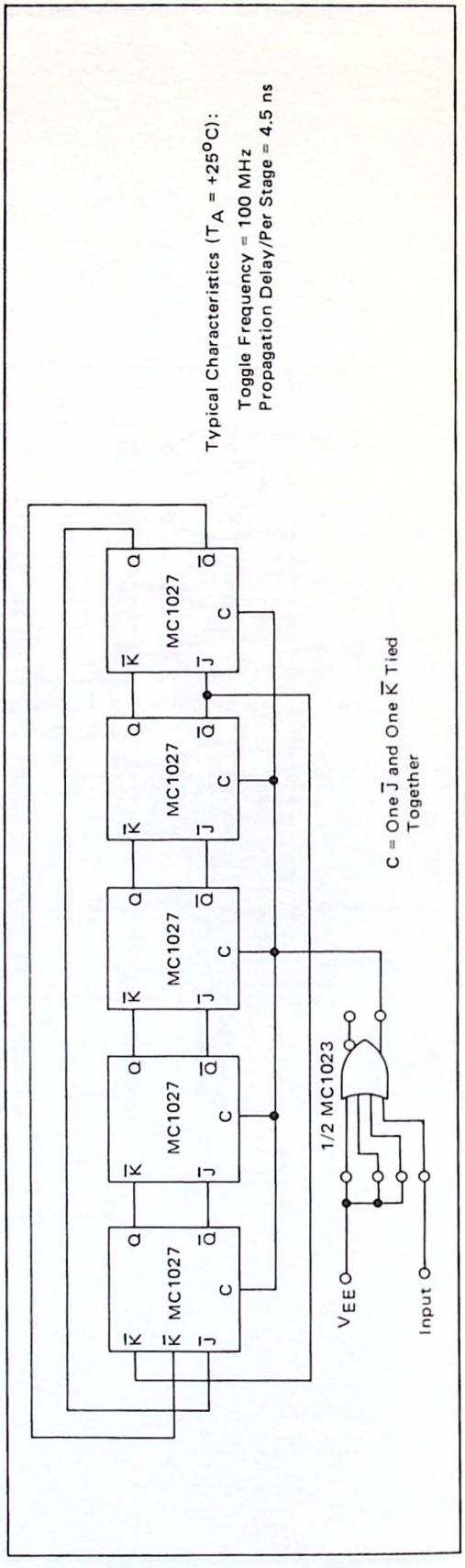
8-14: MECL II 50 MHz + N Counter



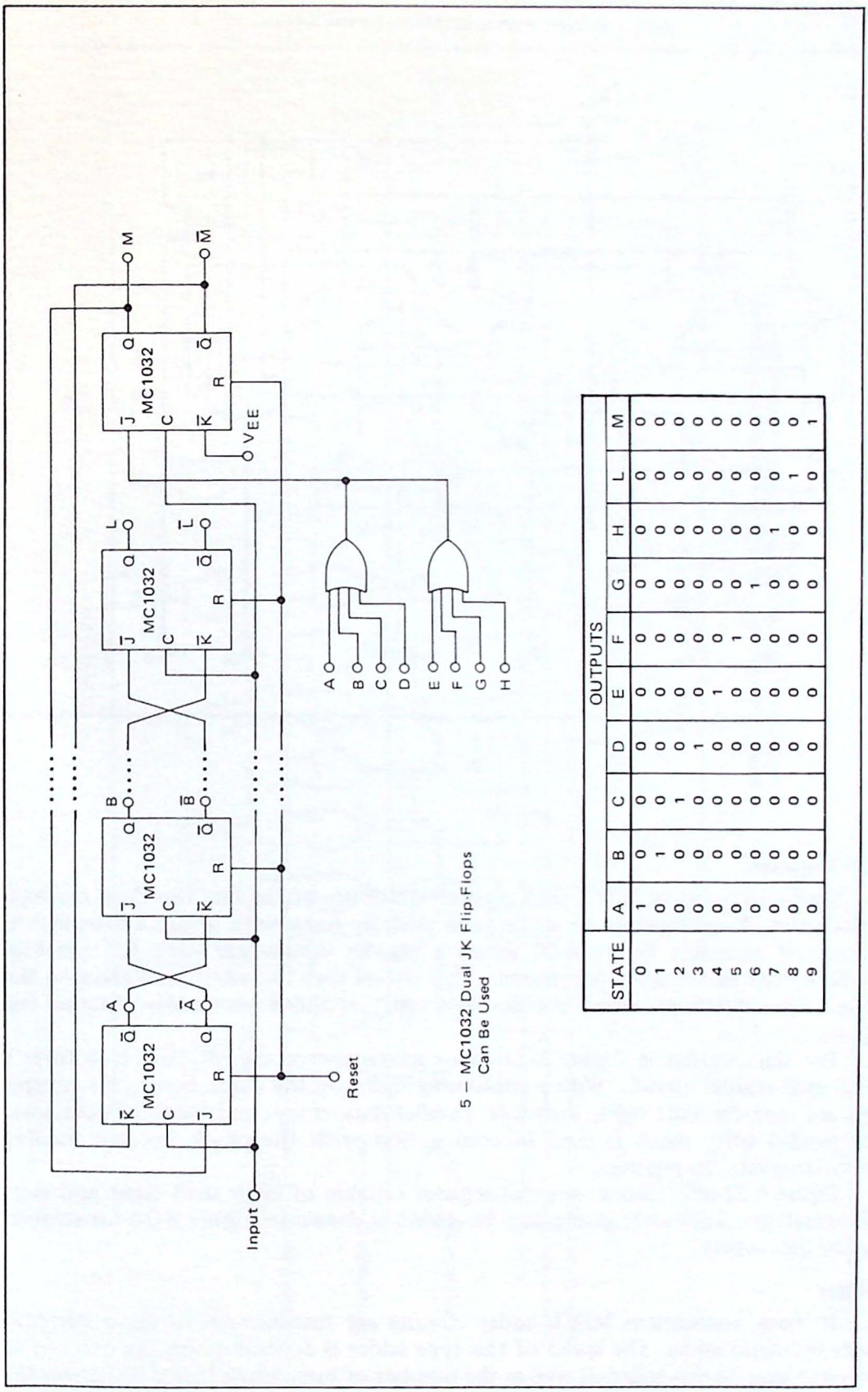
8-15: High Speed MECL III BCD Programmable Counter



8-16: MECL II Decade Ring Counter



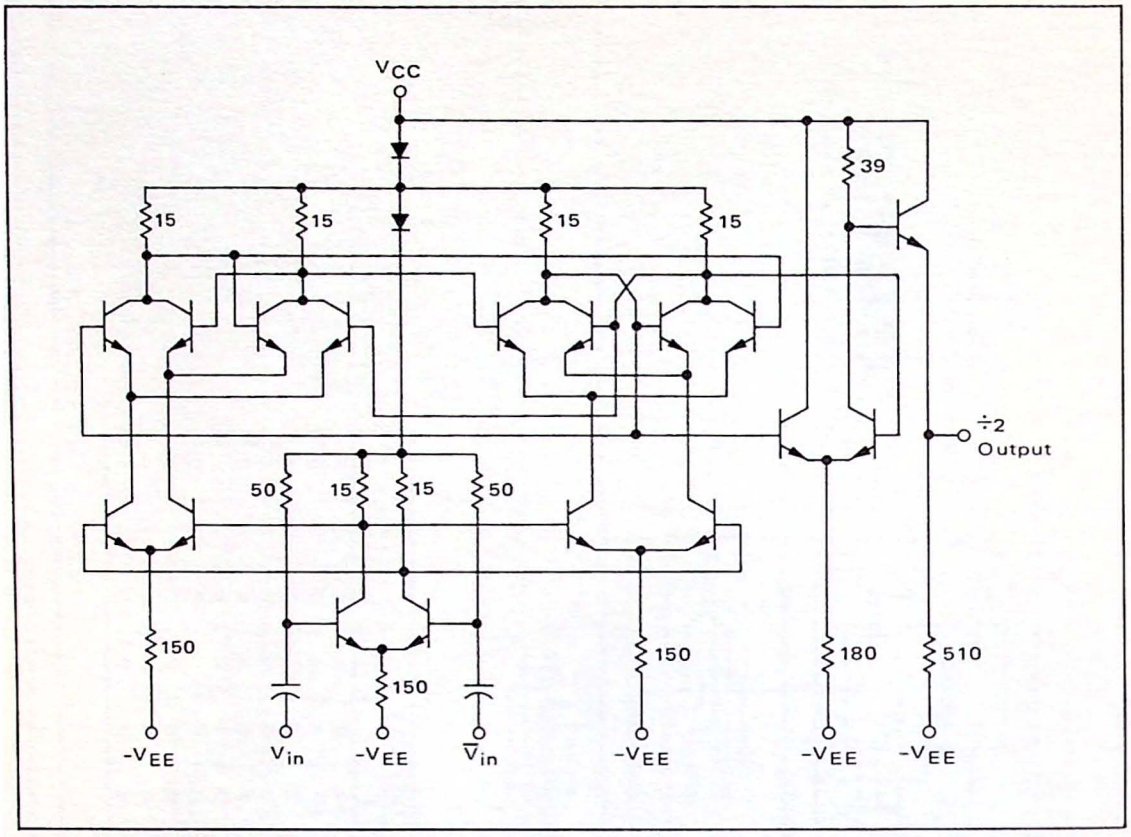
8-17: MECL II 100 MHz Decade Ring Counter



STATE	OUTPUTS									
	A	B	C	D	E	F	G	H	L	M
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1

8-18: Self Correcting Decade Ring Counter

8-19: Functional High-Speed Binary Divider Circuit



Shift Registers

Similar to counters, MECL shift registers make use of the fast flip-flops for high performance. These registers are often used as delay lines, with delays controlled to nanosecond accuracy. Figure 8-20 shows a register commonly used for serial-to-parallel and parallel-to-serial conversions. This circuit uses the additional gates on the set and reset inputs to permit parallel data entry without previously clearing the register.

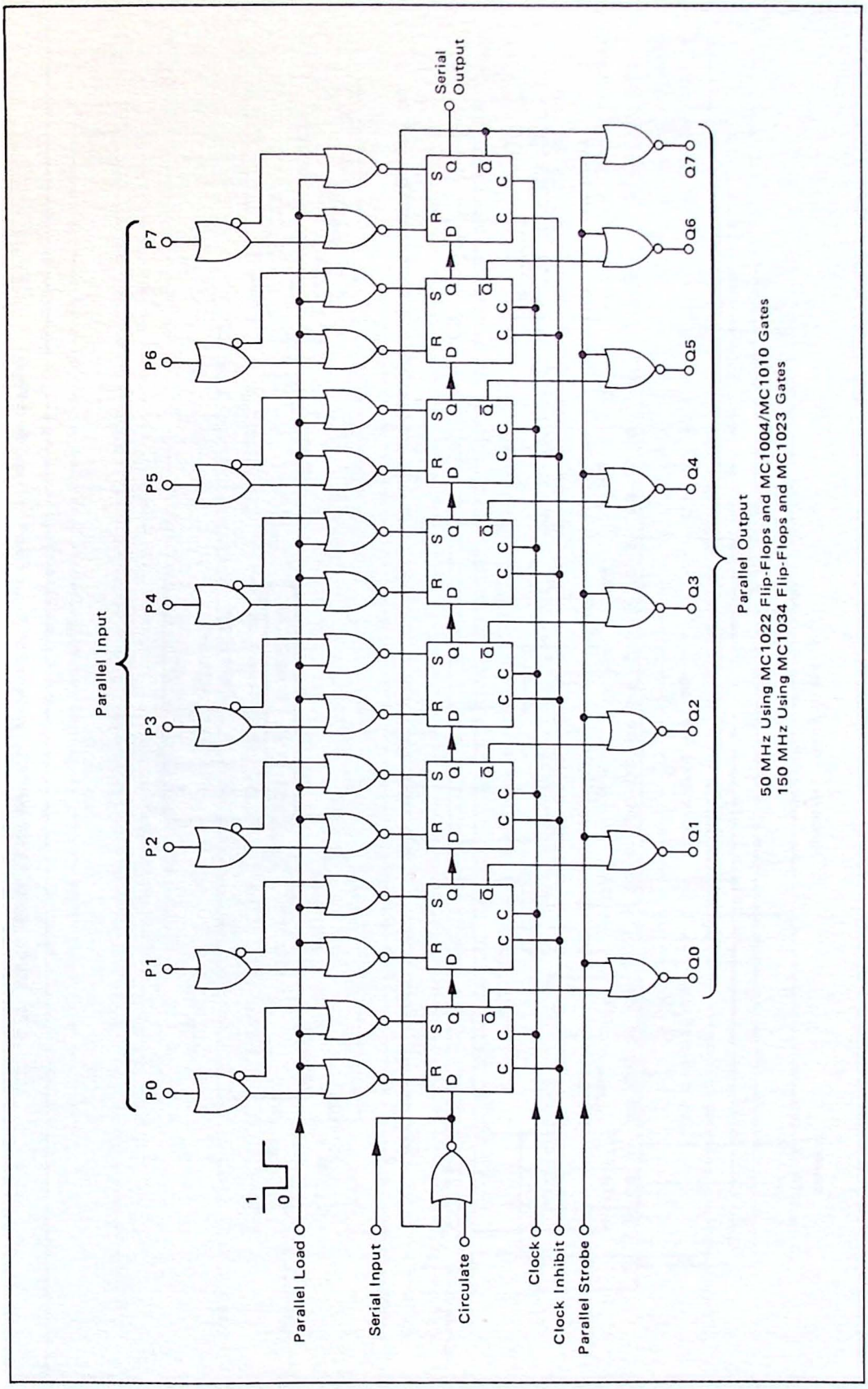
The shift register in Figure 8-21 takes advantage of the MC10141 to form a 16-bit shift register circuit. With a continuing signal on the clock input, the control lines are used for shift right, shift left, parallel data entry, and inhibit operations. The parallel entry mode is used in conjunction with the clock line for loading information into the register.

Figure 8-22 illustrates a universal register capable of both shift right and shift left operations. Additional gating may be added as shown in Figure 8-20 for strobed parallel data inputs.

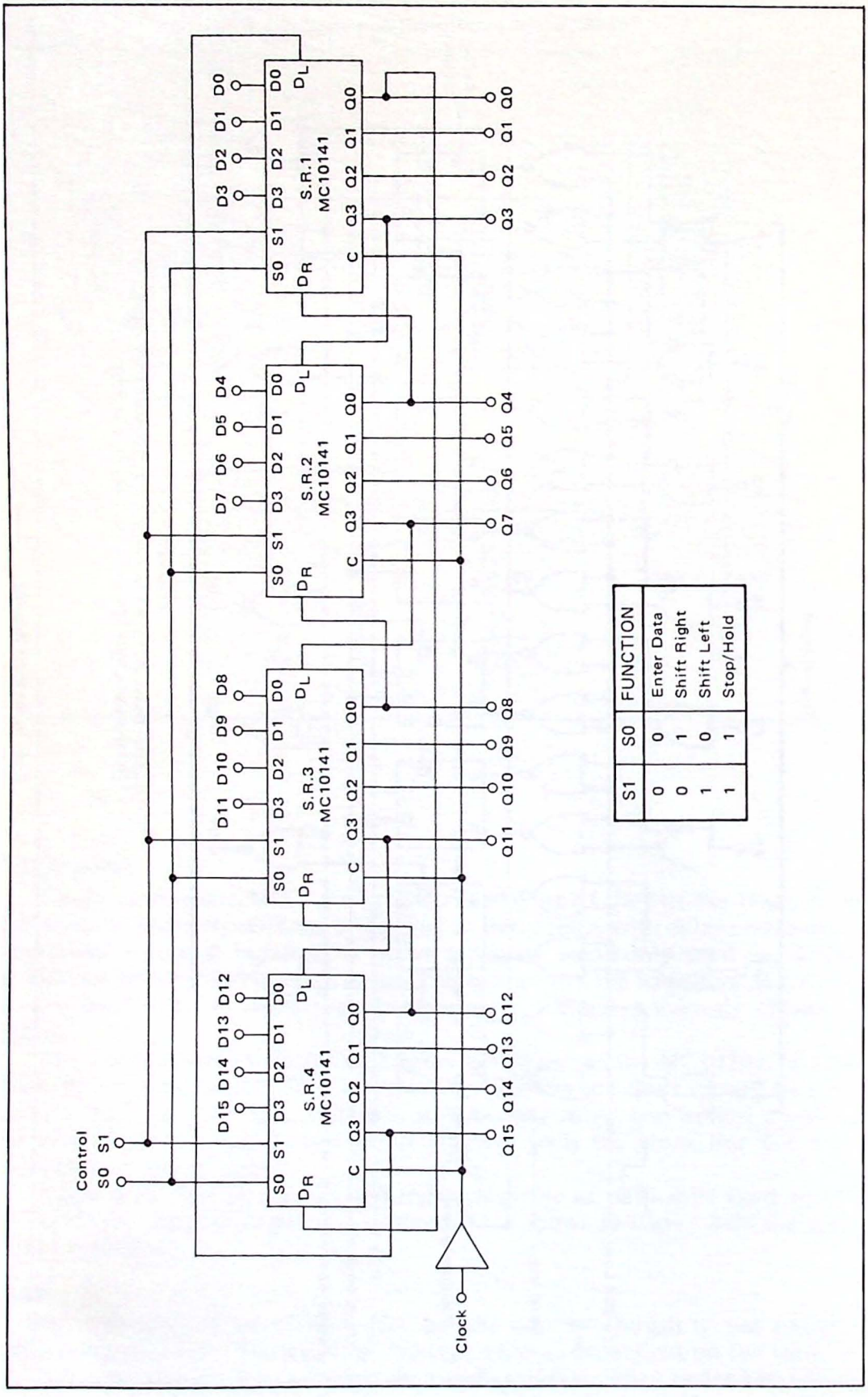
Adders

In many applications MECL adder circuits are fast enough to use a standard ripple-technique adder. The speed of this type adder is dependent on the carry-in to carry-out time of the adder, as well as the number of bits. When faster add times are

(Continued on Page 188)

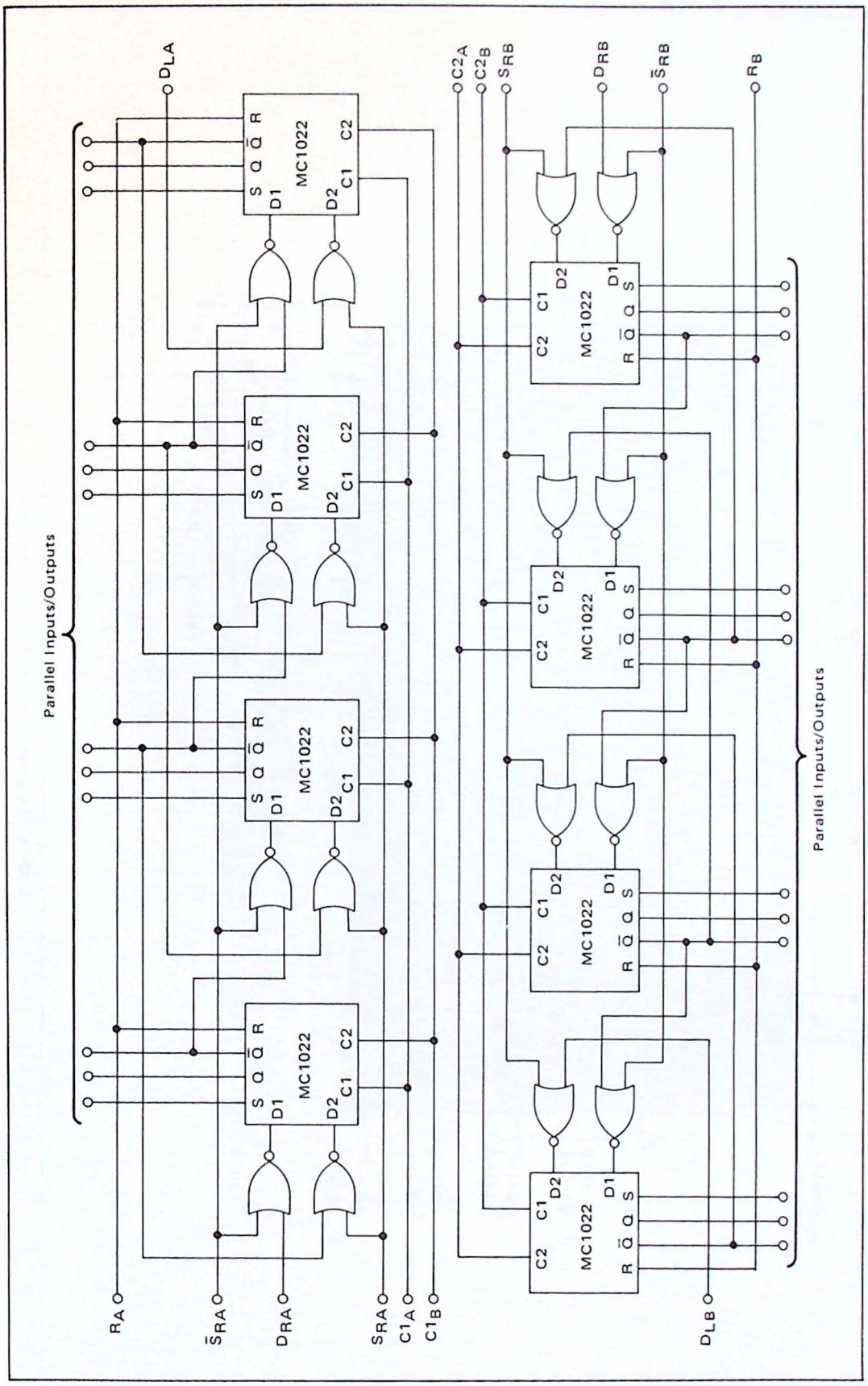


8-20: 8-Bit Shift Register

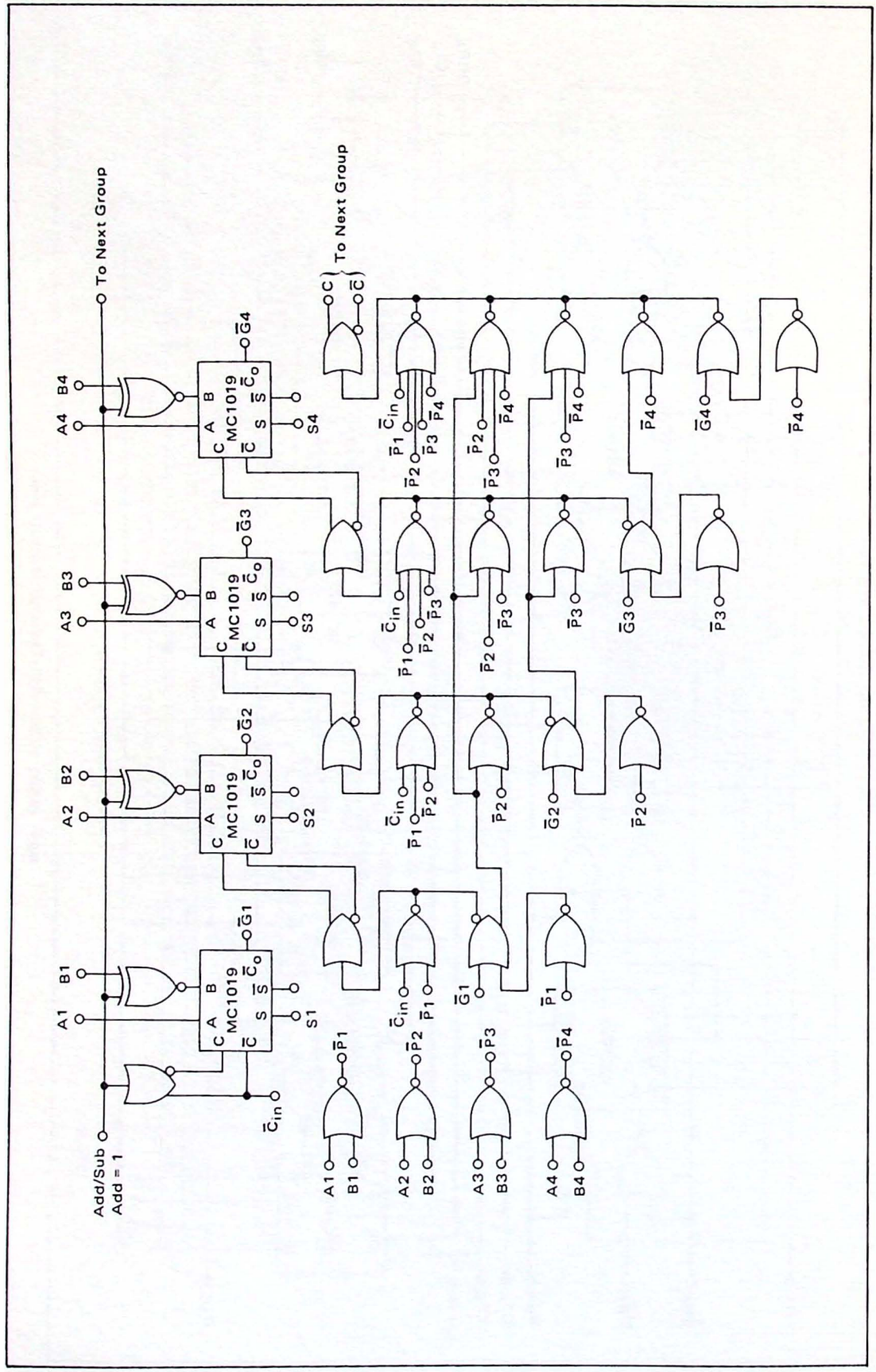


S1	S0	FUNCTION
0	0	Enter Data
0	1	Shift Right
1	0	Shift Left
1	1	Stop/Hold

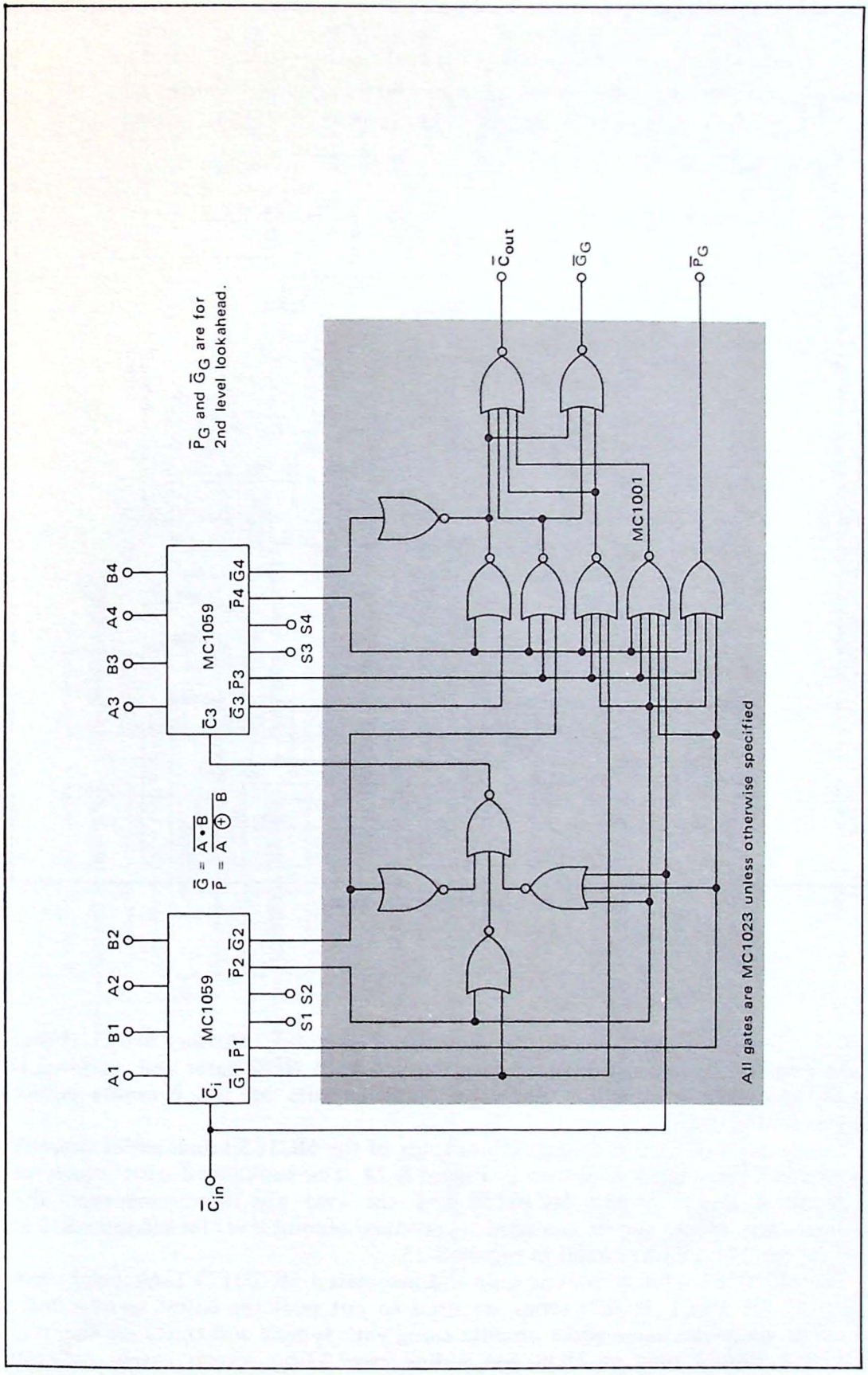
8-21: MECL 10,000 16-Bit Shift Register With End-Around Shift-Left and Shift-Right



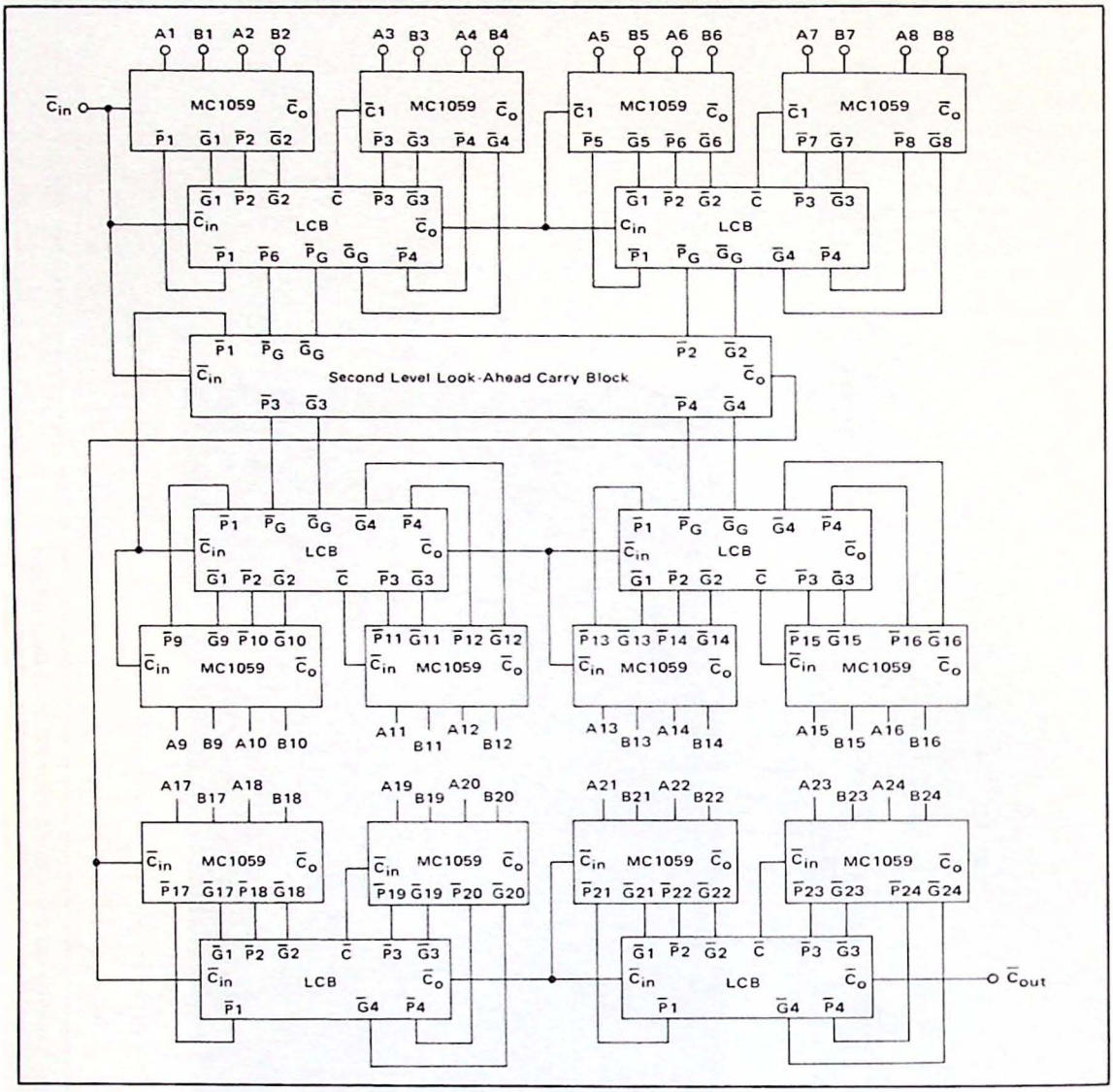
8-22: MECL II Dual 4-Bit Universal Shift Register



8-23: MECL II Add/Subtract With Lookahead Carry



8-24: Look-Ahead Carry Block With MECL II Dual Adders



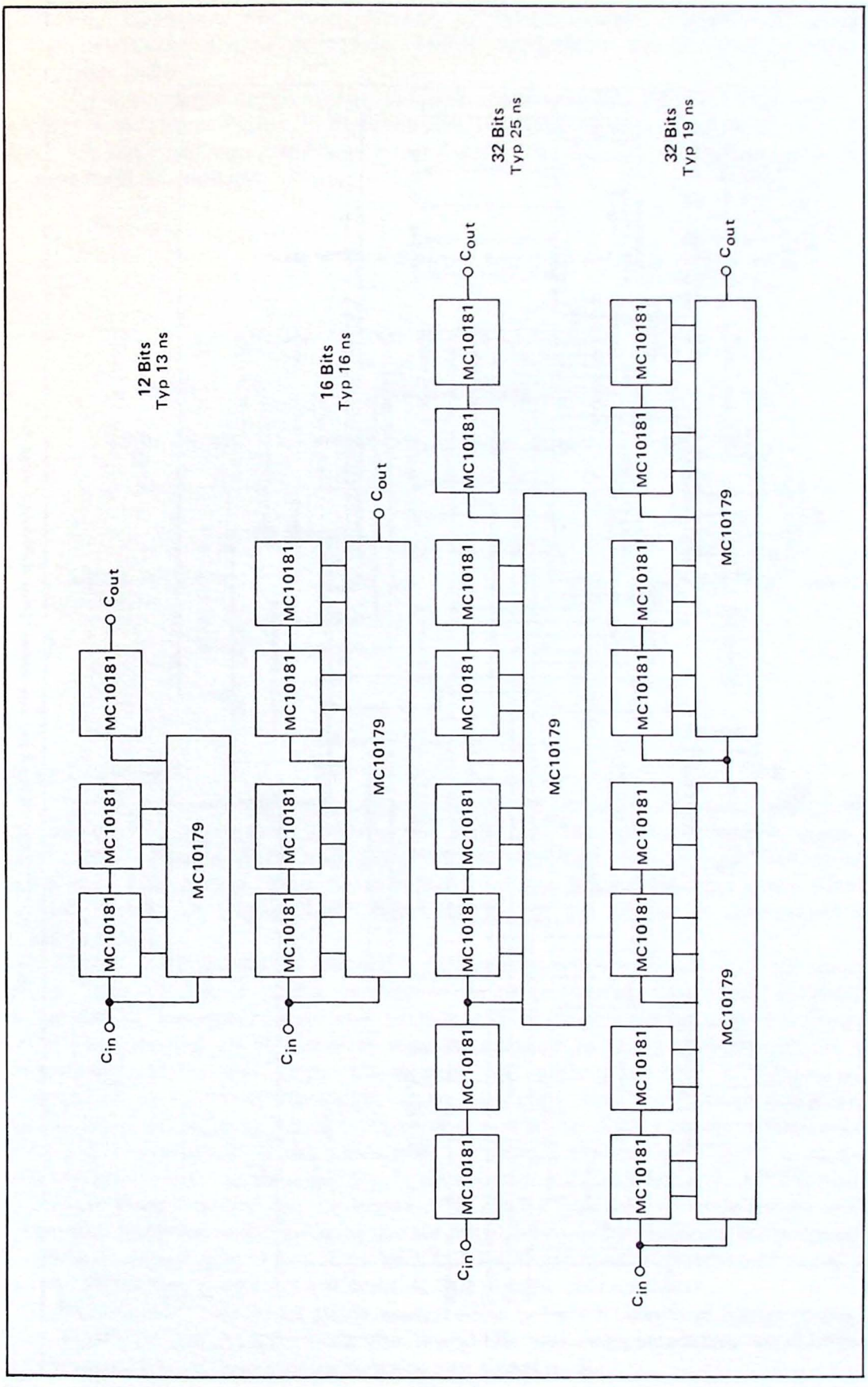
8-25: 24-Bit Look-Ahead Carry Adder

required, a lookahead-carry circuit may be used. Figure 8-23 shows a MECL II four bit adder block. The propagate function is derived with NOR gates and carry-out is used for the generate function. Exclusive NOR circuits on the B inputs permit adding or subtracting.

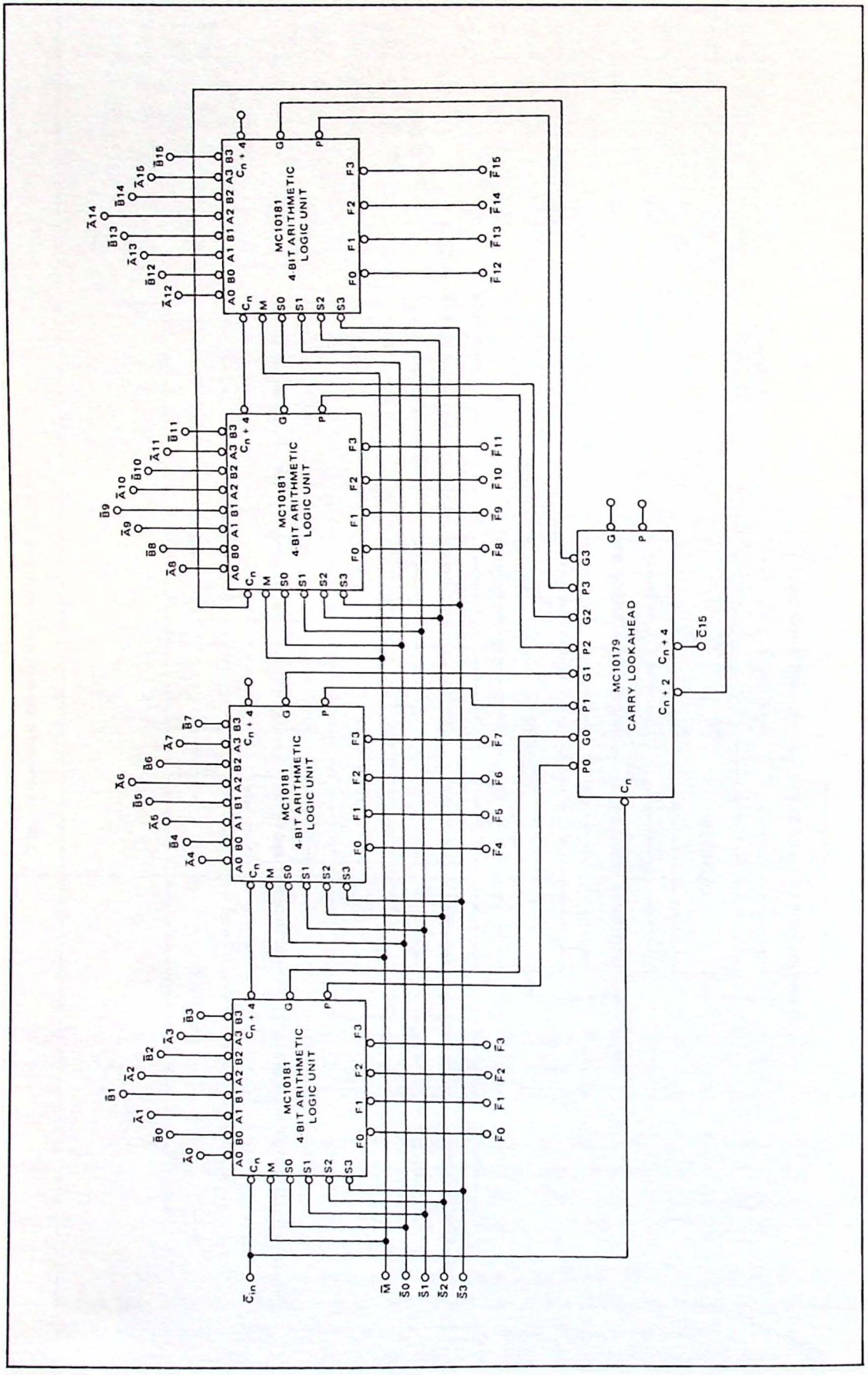
The generate (G) and propagate (P) outputs of the MC1059 dual adder simplify the lookahead carry block as shown in Figure 8-24. The lookahead carry block for this circuit is similar to the MC10179 and the two are interchangeable. The lookahead carry blocks can be cascaded to produce second level lookahead carry as shown for the 24-bit adder circuit in Figure 8-25.

The MC10181 4-bit arithmetic unit and associated MC10179 lookahead carry block from the MECL 10,000 series are used to cut package count significantly. Figure 8-26 illustrates some adder circuits along with typical add times for the total circuit. The typical time of 19 ns for adding two 32-bit words (using only 10

(Continued on Page 191)



8-26: Arithmetic Operations With MECL 10,000

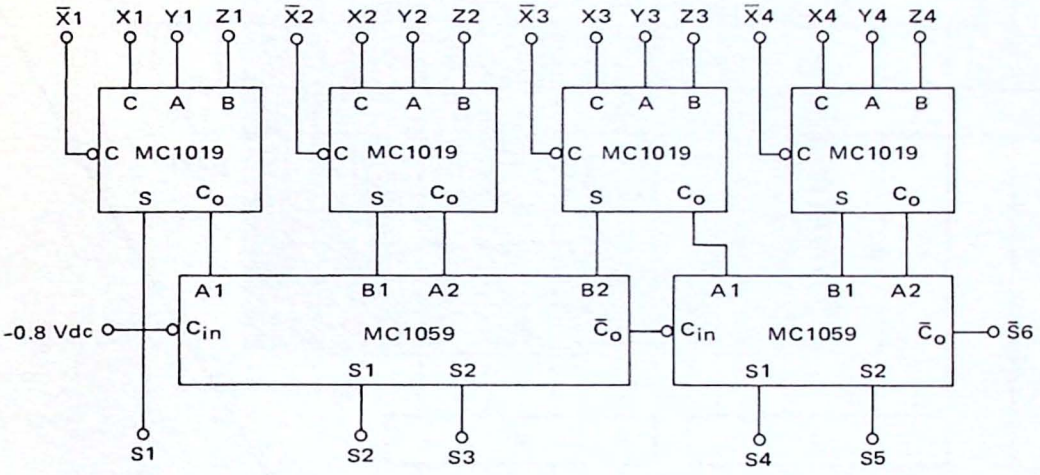


8-27: MECL 10,000 16-Bit Full Look-Ahead Carry Arithmetic Logic Unit

packages) illustrates the performance of MECL adders. Figure 8-27 shows the interconnections for a complete 16-bit arithmetic circuit with second level lookahead carry.

For specialized applications, three numbers may be added simultaneously using a carry/save adder. Figure 8-28 illustrates this type of adder using MECL II circuits. Both the sum and carry outputs from the first level adder are used as inputs for the second level of addition.

8-28: MECL II 3 Number 4-Bit Carry/Save Adder



Code Converters

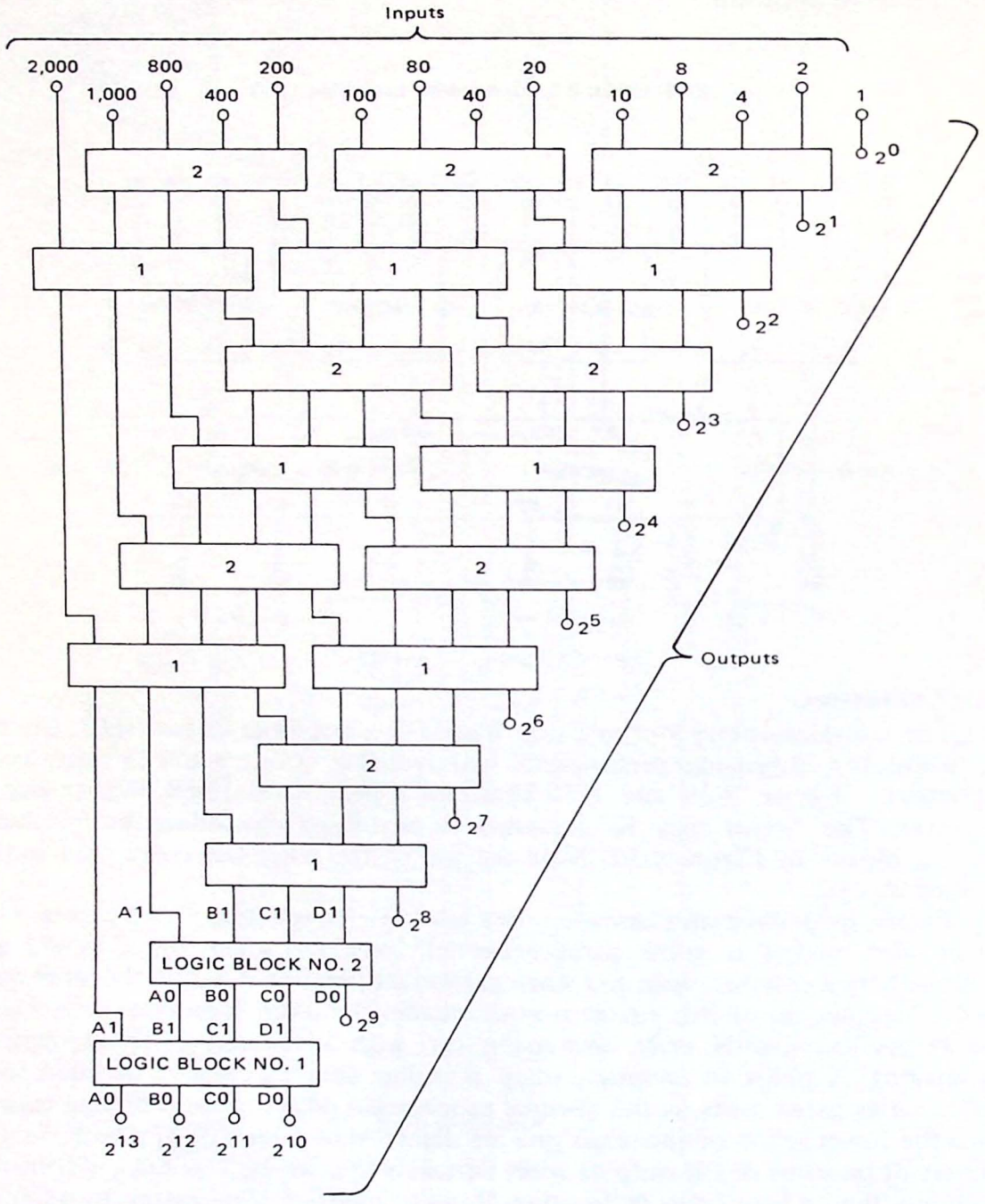
The complementary outputs and Wired-OR capabilities of the MECL circuits are useful for improving performance and reducing circuit count in many code converters. Figure 8-29 and 8-30 illustrate a high speed ripple BCD-to-binary converter. The circuit may be extended to any length by adding the two basic building blocks of Figure 8-30. Note the use of the Wired-OR connection in the building blocks.

Figure 8-31 illustrates cascaded data selectors for selecting 1 of 32 lines. This circuit also makes a good parallel-to-serial converter when the C inputs are controlled by a counter chain and when parallel information is put on the input data lines. The converse of this circuit is made possible by using decoder circuits which give binary-to-one-of-N code conversion (or, with a counter, a serial-to-parallel conversion). A point to consider, when cascading data selectors or decoders with MECL series gated parts, is the unequal propagation delays of the differing inputs. Since the lower levels of the series gate are slightly slower than the top level, a spike may result on some of the outputs while switching the circuit. This spike is normally much less than a gate delay in duration. It can be nullified, if necessary, by adding a faster gate in series with the appropriate input leads or by sampling the outputs after the longest delay-path time. The MECL 10,000 series multiplexers and decoders do not use series gating and do not exhibit this output characteristic.

Figures 8-32 and 8-33 show conversions between Gray and binary codes. The Gray-to-binary coding uses both the Wired-OR and complementary gate outputs to give a maximum of two gate delays for any signal path.

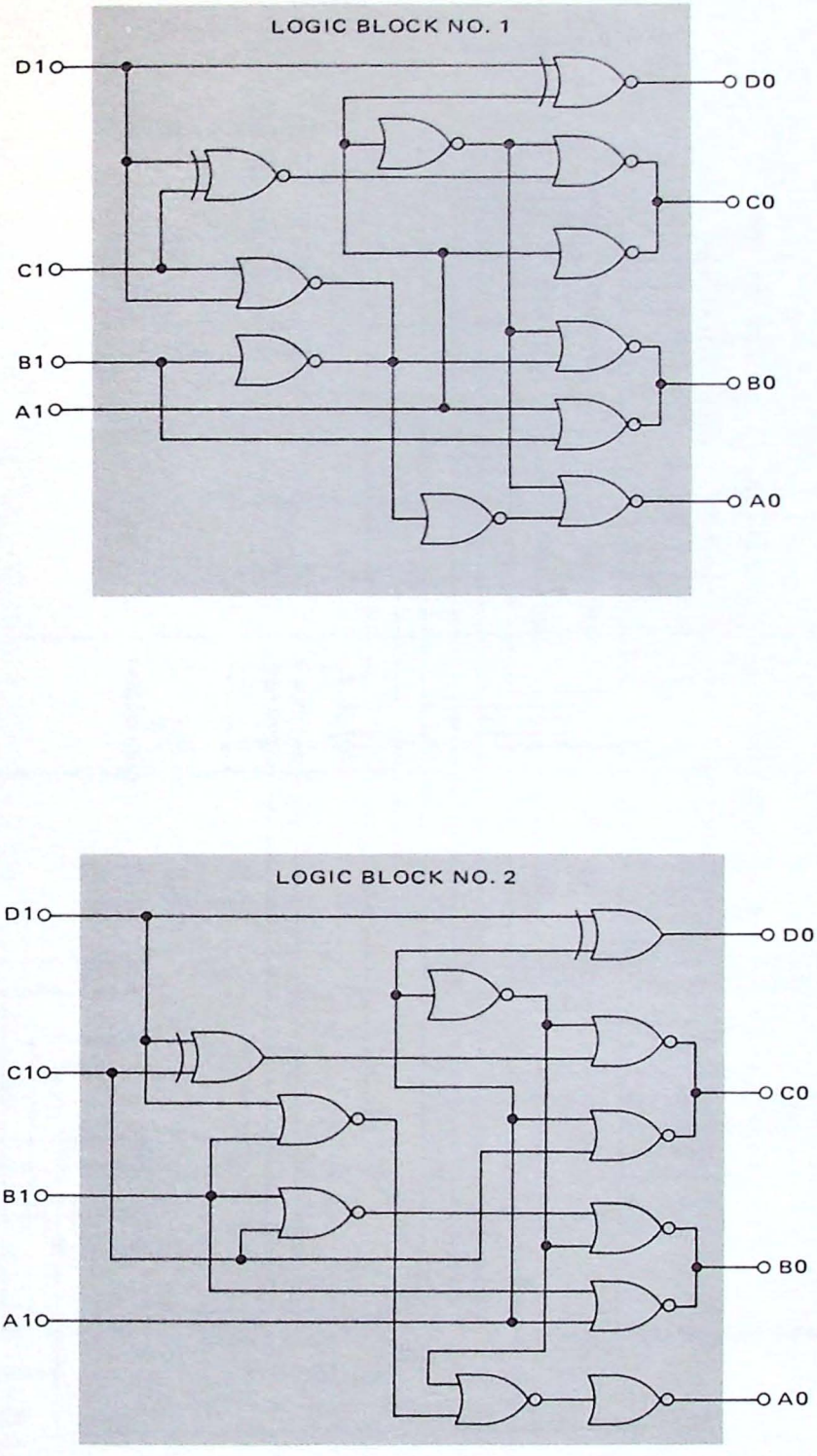
(Continued on Page 196)

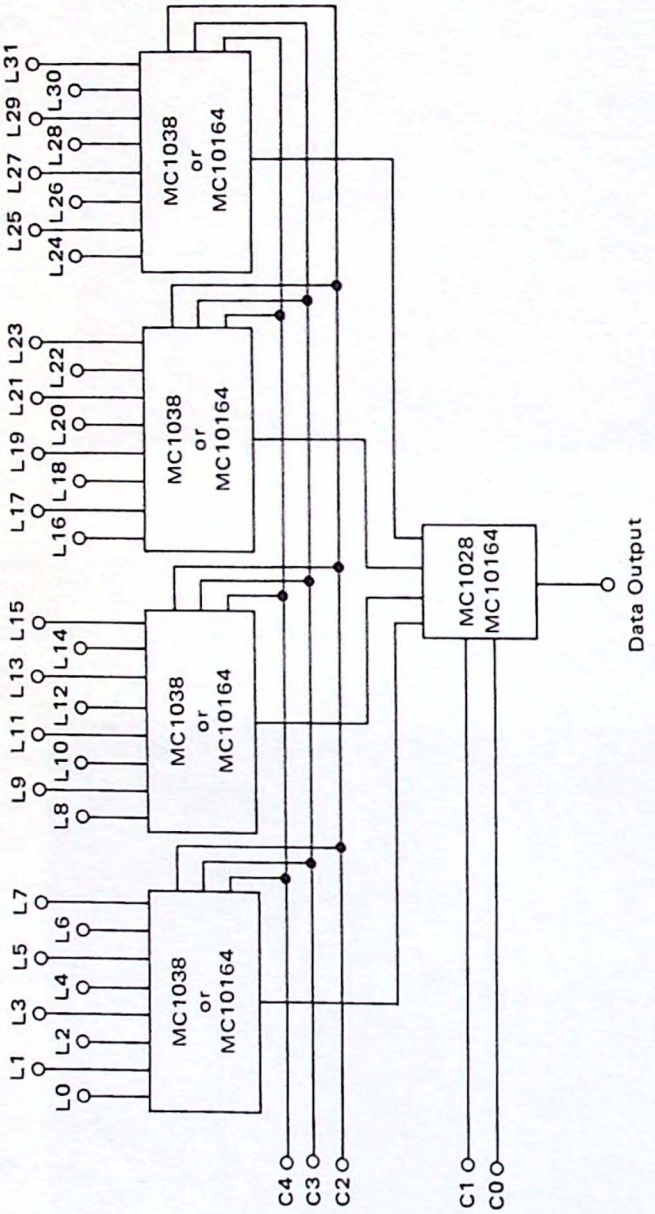
8-29: Ripple BCD to Binary Converter



Max Ripple Delay for 14-Bits of BCD to 12 Binary Bits: 140 ns for MECL II

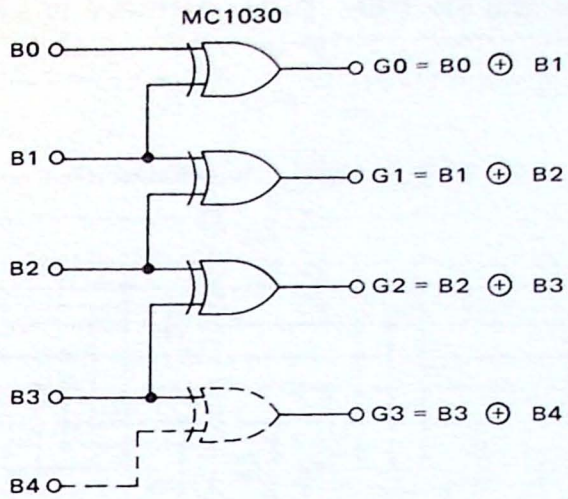
8-30: MECL II BCD to Binary Converter Logic Blocks





8-31: 32 Channel Data Selector Array with Cascaded Data Selectors

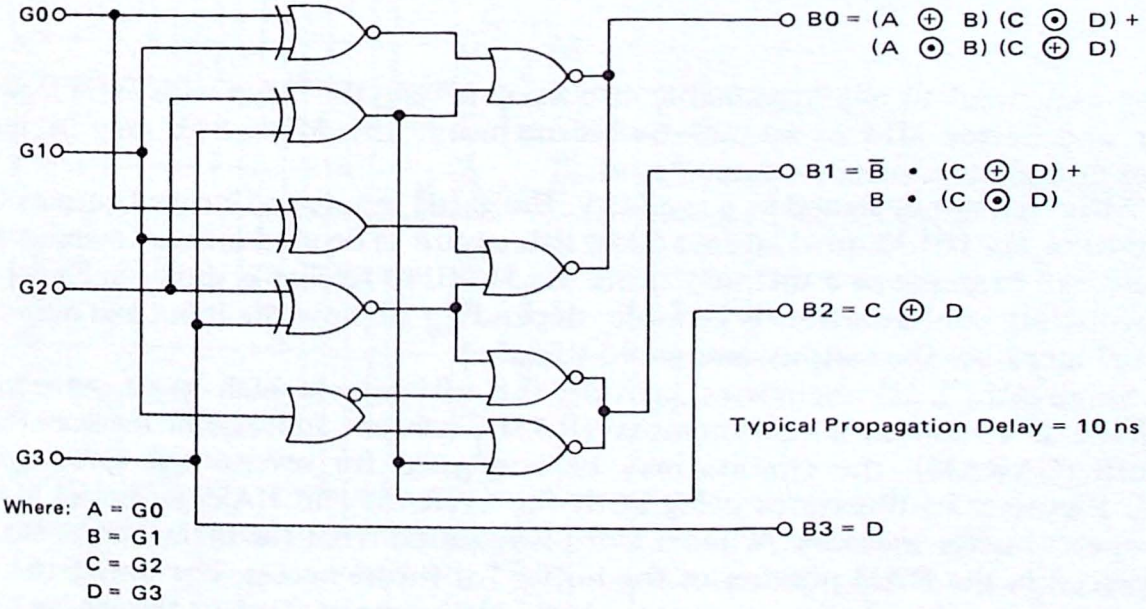
8-32: MECL II Binary to Gray Code Converter



Typical Propagation Delay = 5 ns

8-33: MECL II Gray to Binary Code Converter

Logic: MC1010, MC1030, MC1031



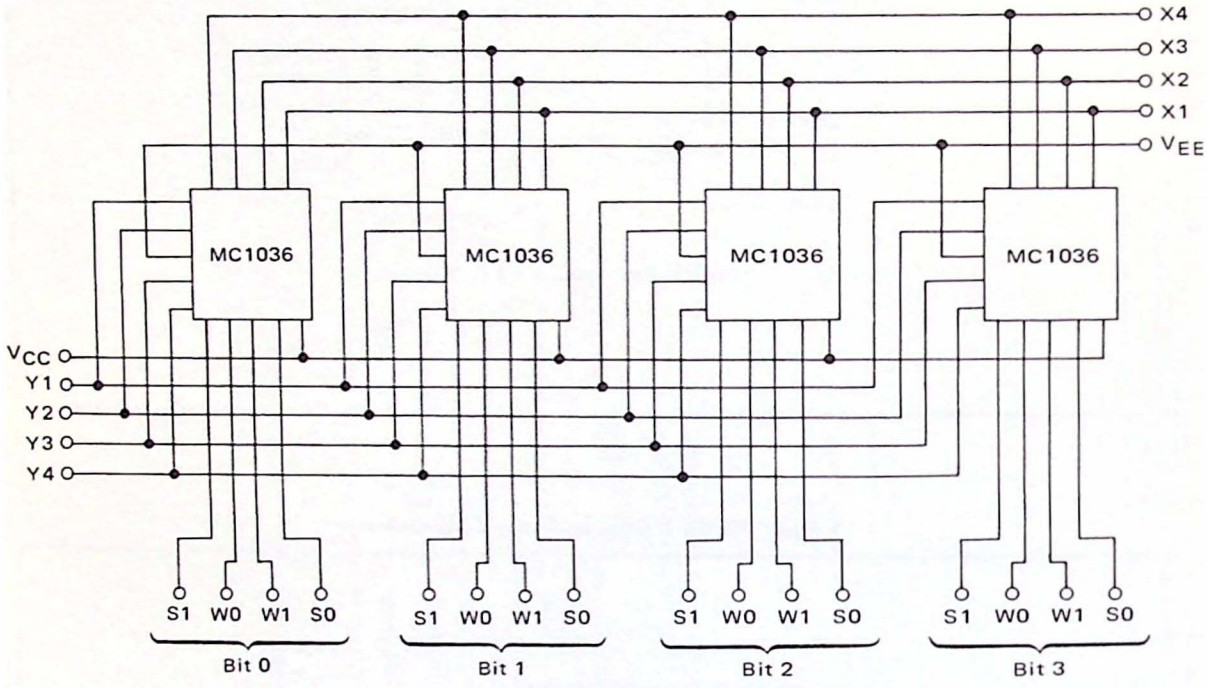
Typical Propagation Delay = 10 ns

Where: A = G0
B = G1
C = G2
D = G3

Memories

While the cost and size of present MECL memories limit their practical use for very large storage, the fast access and write times can speed-up system operation when these circuits are used for scratch-pad or temporary storage memories. Figure 8-34 illustrates the use of the MC1036 16-bit memory in such a circuit. The circuit

8-34: MECL II 16-Word by 4-Bit Memory

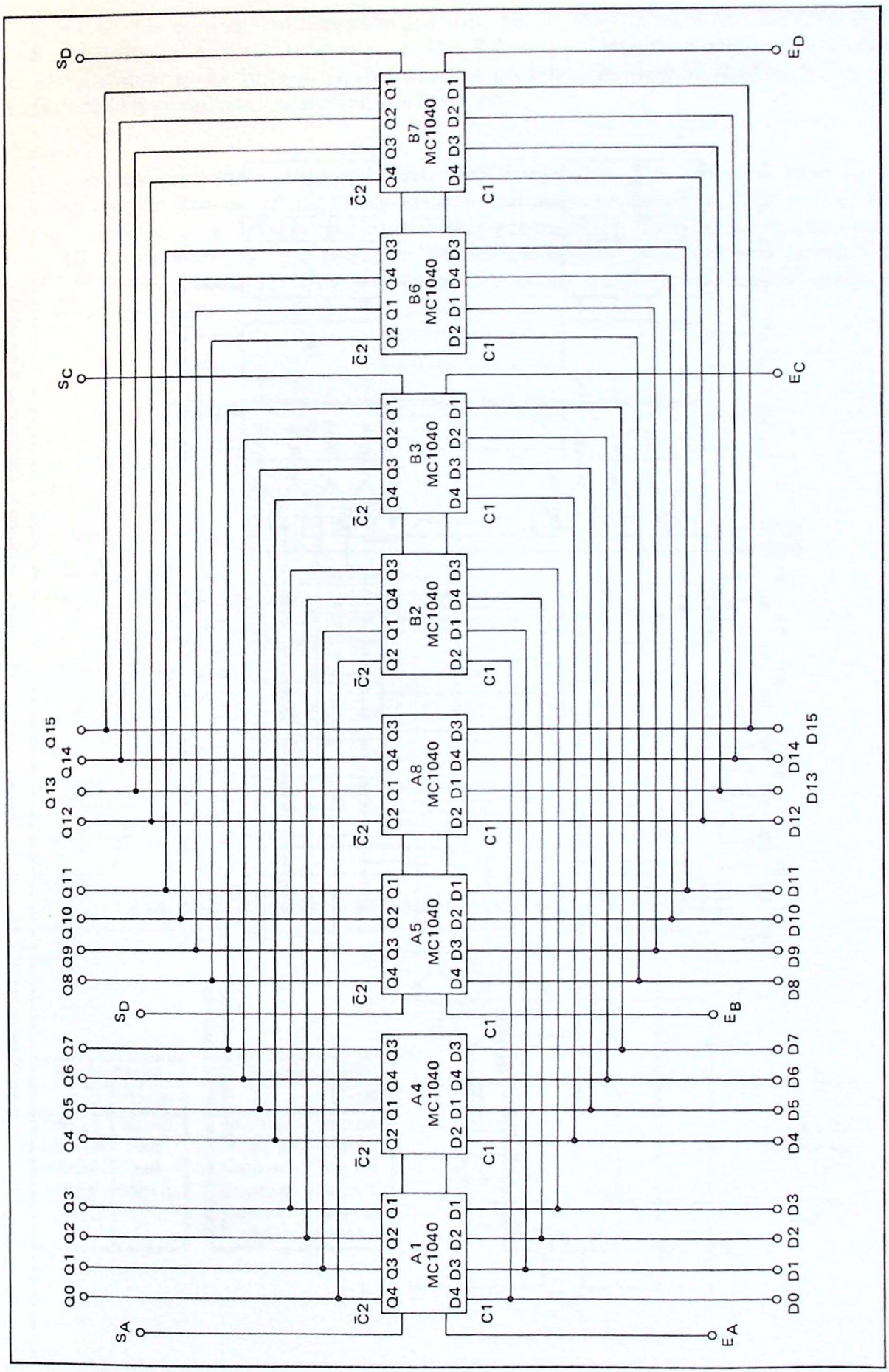


can be expanded to any reasonable size by decoding the input with extra logic. The larger and faster MECL 10,000 64-bit memory, the MC10140, may be used in similar circuits for lower package count.

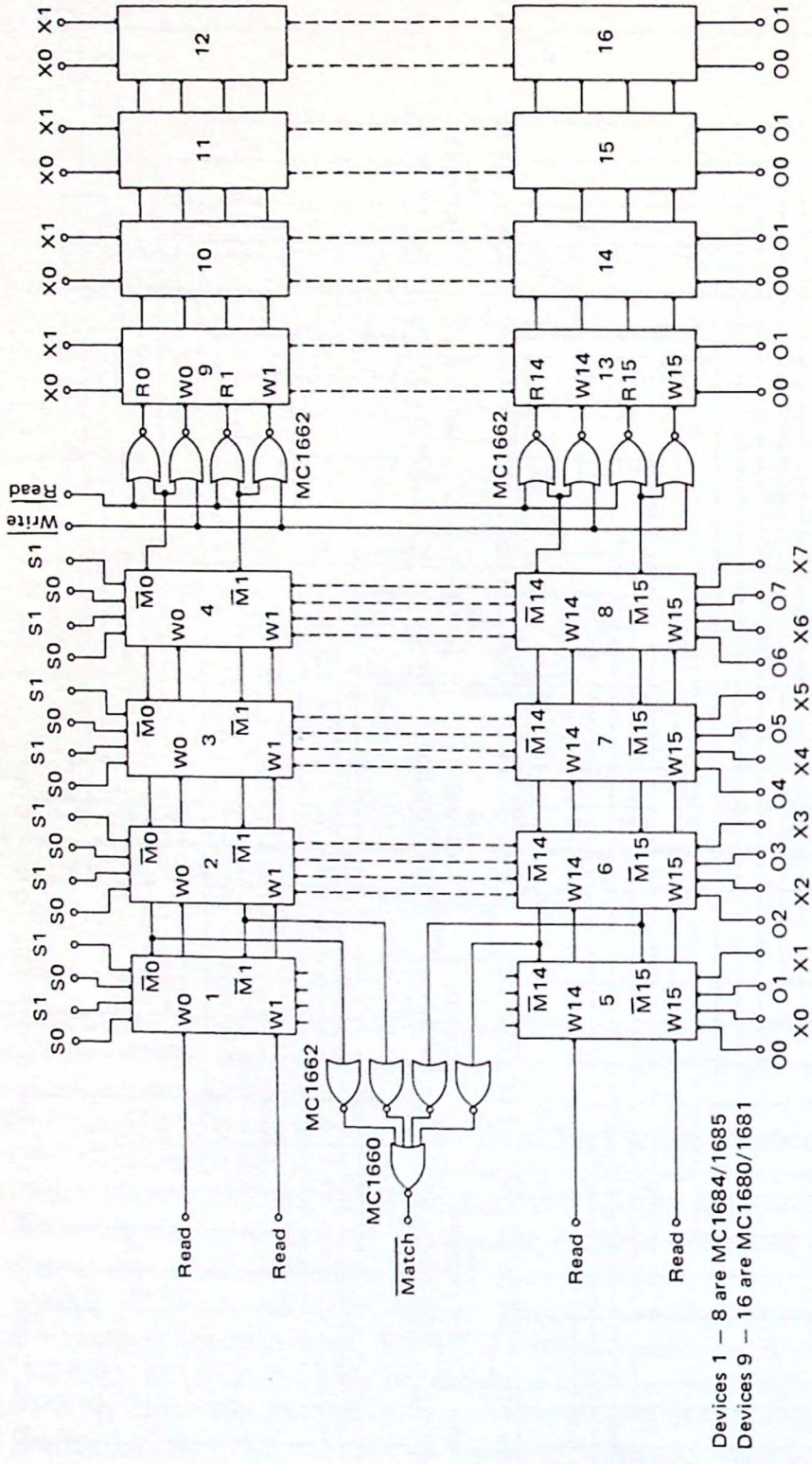
Although not designed as a memory, the gated inputs and strobed outputs of the MC1040 or MC10133 quad latches allow this circuit to be used in many memory applications. An example of a memory using the MC1040 latches is shown in Figure 8-35. The word/bit configuration is flexible, depending on how the input and outputs are selected and how the outputs are wired together.

Small MECL III memories provide the ultimate in high speed performance. Available as a random access memory (RAM), content addressable memory (CAM), or both (CARAM), the circuits may be combined for several high speed memory types. Figure 8-36 illustrates using both the CARAM and RAM memories in a very high speed buffer memory. When a word is required from the main storage memory, it is placed in the RAM portion of the buffer for future access. The word's address in mass storage is placed in a content addressable memory (tied to the random access section), thereby allowing words to be addressed by their mass storage location during one cycle time of the buffer memory. As the address of the desired word is

(Continued on Page 199)



8-35: Dual 8-Bit 2-Address Latch/32-Bit 6 ns MECL II Memory



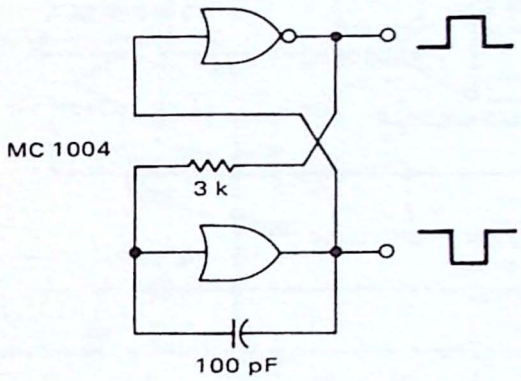
8-36: CAM/RAM High Speed Buffer Memory (MECL III) 64-Word by 2-Bit RAM–16-Word by 8-Bit CAM

presented to the content addressable section, the CAM will indicate (in one cycle time) whether or not the address is in the CAM, and whether or not the desired word is available in the buffer. If the word is present, the desired read and/or write function can be performed at buffer RAM speeds.

Oscillators

Oscillators are easily designed with MECL circuits. The simplest high speed oscillators are formed by an odd number of NOR gates arranged to form a ring. The oscillation frequency is determined by the gate propagation delay and the number of gates. RC timing networks are used for slower oscillators as shown in Figures 8-37 and 8-38. Both of these circuits give complementary outputs and a good range of oscillation frequencies.

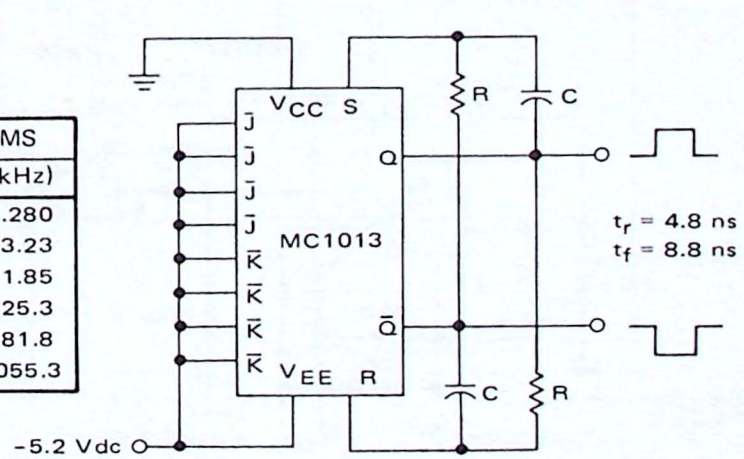
8-37: MECL II Astable Multivibrator with Gates and RC Timing



8-38: MECL II Astable Multivibrator with JK Flip-Flop and RC Timing

R = 3 k OHMS	
C	f (kHz)
0.01 μF	16.113
0.001 μF	150
360 pF	405
100 pF	1361.3

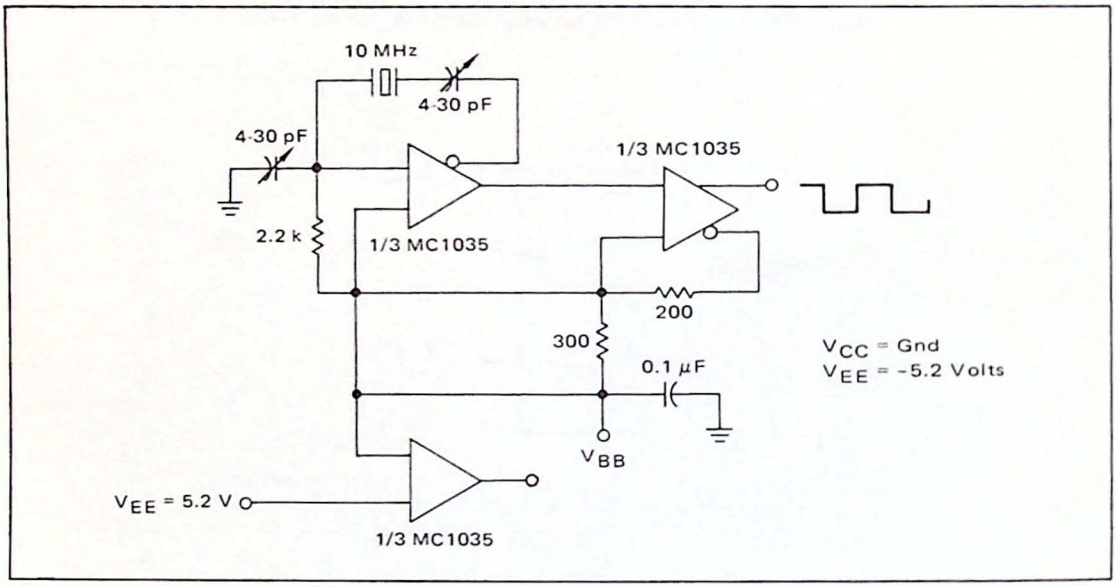
R = 2 k OHMS	
C	f (kHz)
0.01 μF	25.280
0.001 μF	233.23
360 pF	621.85
100 pF	2025.3
24 pF	6481.8
10 pF	10055.3



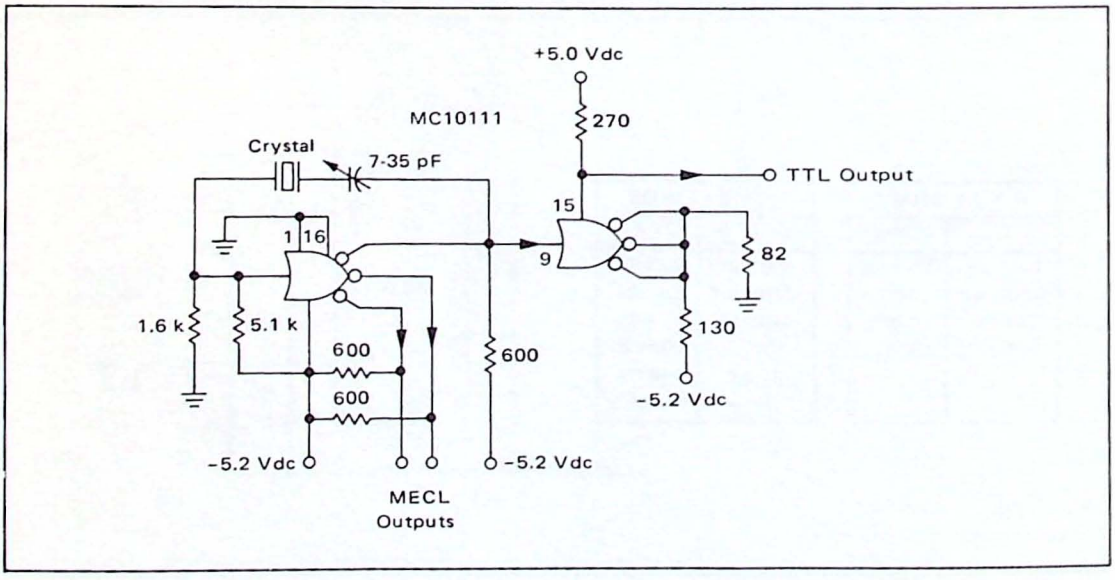
Crystal controlled oscillators are required when tighter frequency control is needed than is practical with the simple RC oscillator. Because of high input impedance and linear operation, any MECL NOR gate may be used in a simple crystal oscillator circuit. However, line receiver circuits are normally used because V_{BB} is available for biasing. Figure 8-39 shows a typical crystal oscillator circuit using the MC1035.

MECL crystal oscillator circuits are often used with TTL designs. By using a resistor in series with the V_{CC} line of a second gate, a MECL crystal oscillator can be converted to a TTL-compatible output, as shown in Figure 8-40. The high speed MECL III circuits are capable of operation beyond practical crystal frequencies. A

8-39: 10 MHz MECL II Crystal Oscillator with Schmitt Trigger



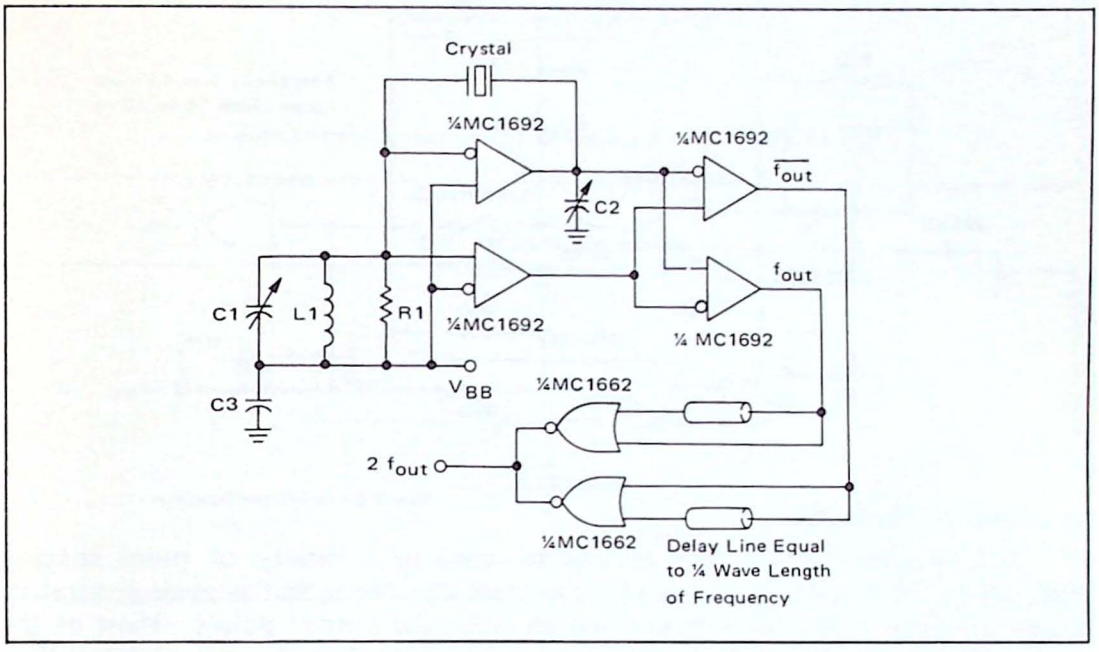
8-40: MECL 10,000 Crystal Oscillator With TTL or MECL Output



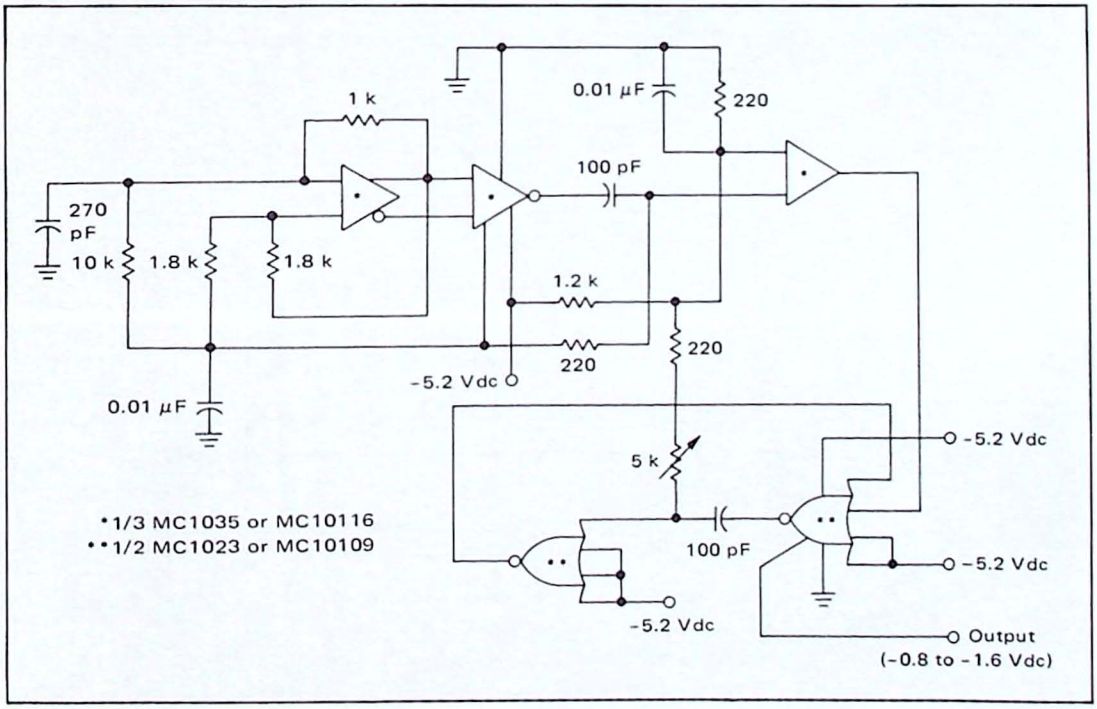
frequency doubler may be used with the crystal oscillator to generate higher frequencies as shown in Figure 8-41. The MC1662 is converted to two one-shot multivibrators by using the proper length delay lines; Wire-ORing the one-shot outputs gives the frequency multiplication.

In addition to oscillators, pulse generators are often required in system design and test equipment. Figure 8-42 illustrates a circuit for constant frequency

8-41: MECL III Crystal Oscillator with Frequency Doubler

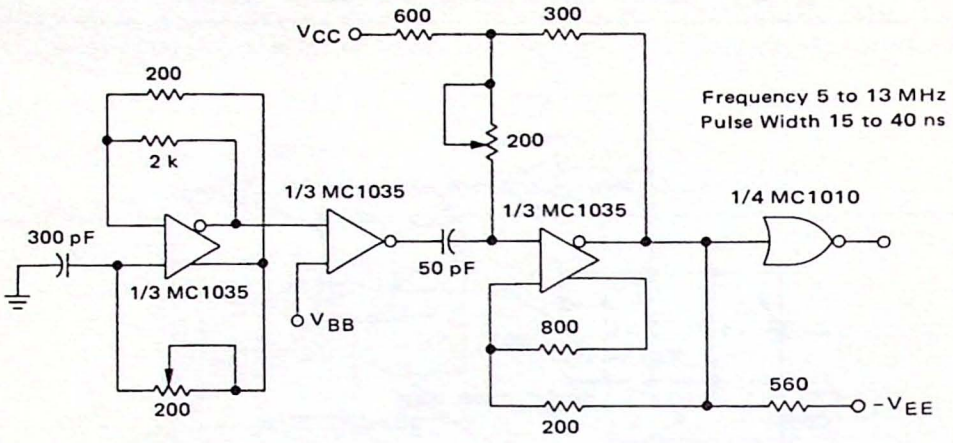


8-42: MECL II/MECL 10,000 Variable Pulse Width Generator



operation with variable pulse width. Figure 8-43 shows a generator with both variable frequency and variable pulse width.

8-43: MECL II Pulse Generator: Variable Frequency and Pulse Width

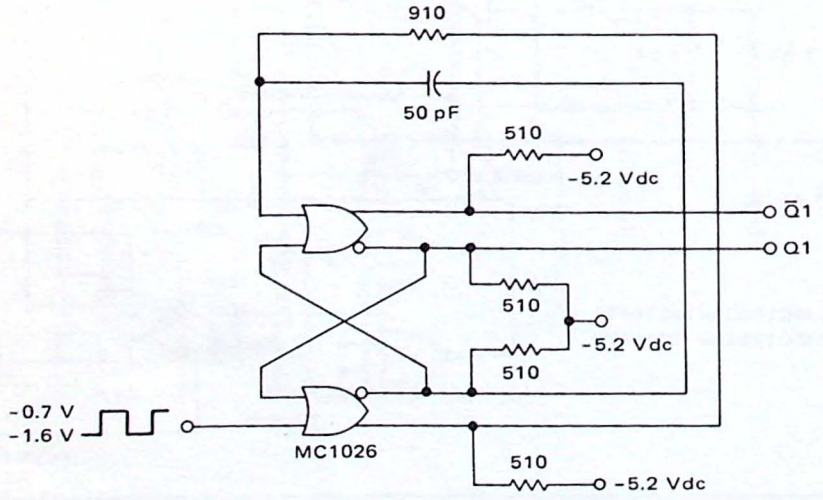


One-Shot Multivibrators

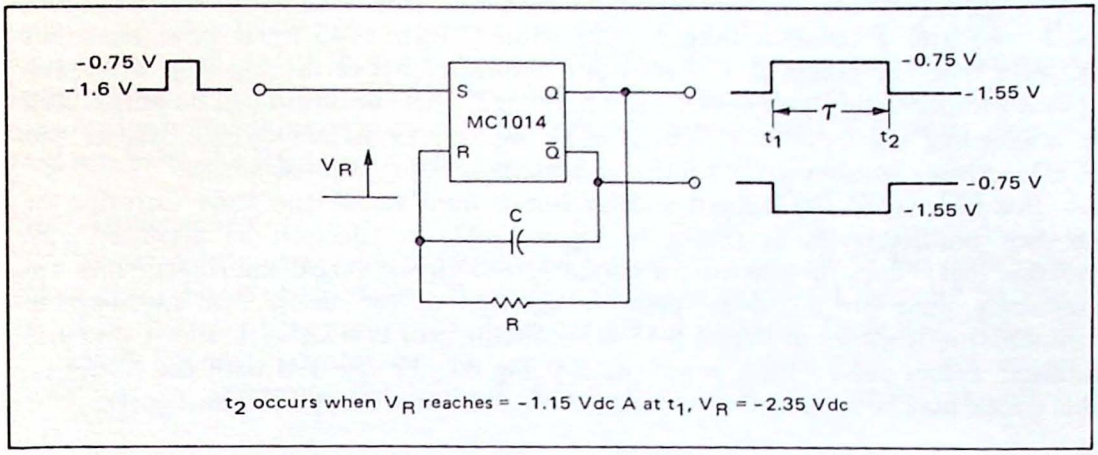
The one-shot multivibrator circuits are used in a variety of pulse shaping applications. These circuits are used both as pulse stretchers, and as pulse generators driven by input pulses differing in duration from the output pulses. Most of the slower circuits use RC timing to determine pulse width; but the use of delay lines gives better results for very narrow pulses.

Figures 8-44, 8-45, and 8-46 illustrate three techniques for shaping pulses. If the input pulse is narrower than the time constant setting, the output in Figure 8-46 will

8-44: Monostable Multivibrator: Constant Output Pulse Width

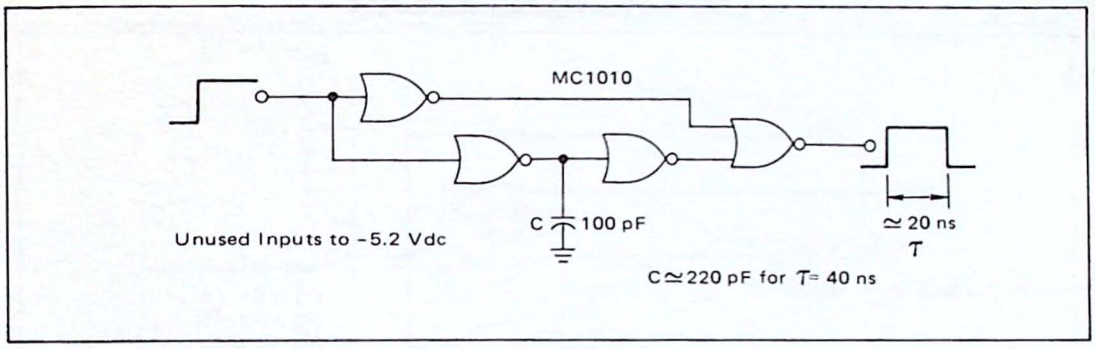


8-45: MECL II One-Shot Multivibrator

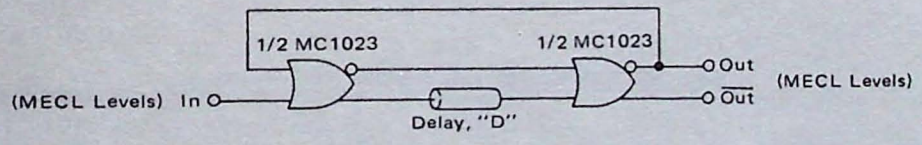


t_2 occurs when V_R reaches = -1.15 Vdc A at t_1, V_R = -2.35 Vdc

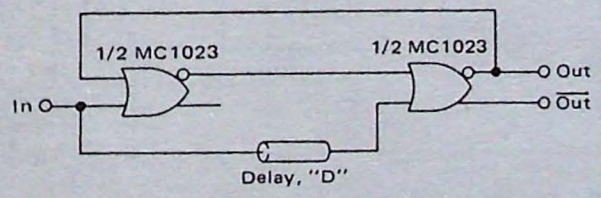
8-46: MECL II Multivibrator



8-47: High Speed Multivibrators



(a) Monostable Multivibrator: Pulse Width Depends Only On Delay "D"

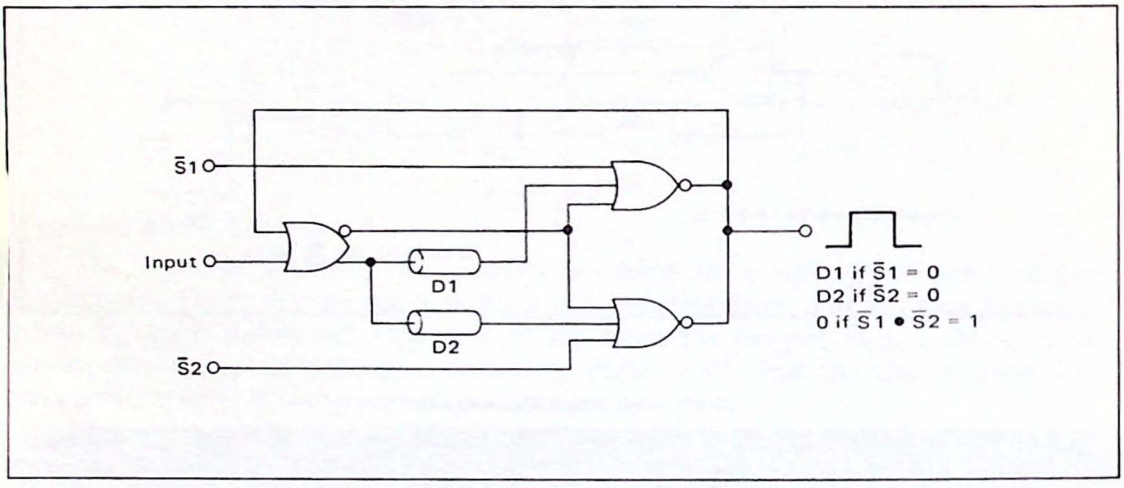


(b) Fast Recovery Monostable Multivibrator: Pulse Width Equals "D" Minus Gate t_{pd}

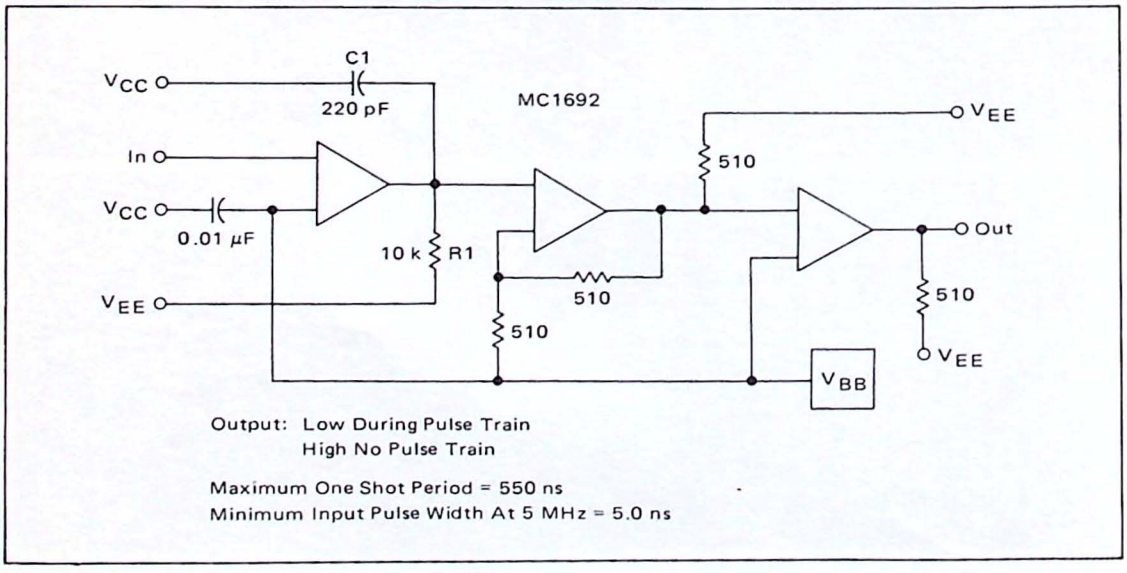
follow the input. The one-shot in Figure 8-44 will accept an input of any pulse width and give a constant output pulse width. Figure 8-45 must have an input narrower than the output and be used as a pulse stretcher or the flip-flop will reach an indeterminate state with both set and reset high. This condition can be eliminated by connecting the input to a $\overline{J}$ input of an MC1013 or similar circuit. Use of the MC1013 gives a constant pulse width out, regardless of input pulse width.

For high speed applications a delay line is used to set the time duration of one-shot multivibrators as shown in Figure 8-47. In addition to commercially available delay lines, lengths of coaxial cable and circuit board microstrip line are commonly used for the delay path. A variation of the delay line monostable multivibrator is shown in Figure 8-48. This circuit uses two delay lines of unequal duration. Either pulse length, or no output pulse, may be selected with the $\overline{S}$ inputs. This circuit may be expanded as necessary with additional delay lines and gates.

8-48: Gated Pulse Width One-Shot Multivibrator



8-49: MECL III Retriggerable One-Shot Multivibrator

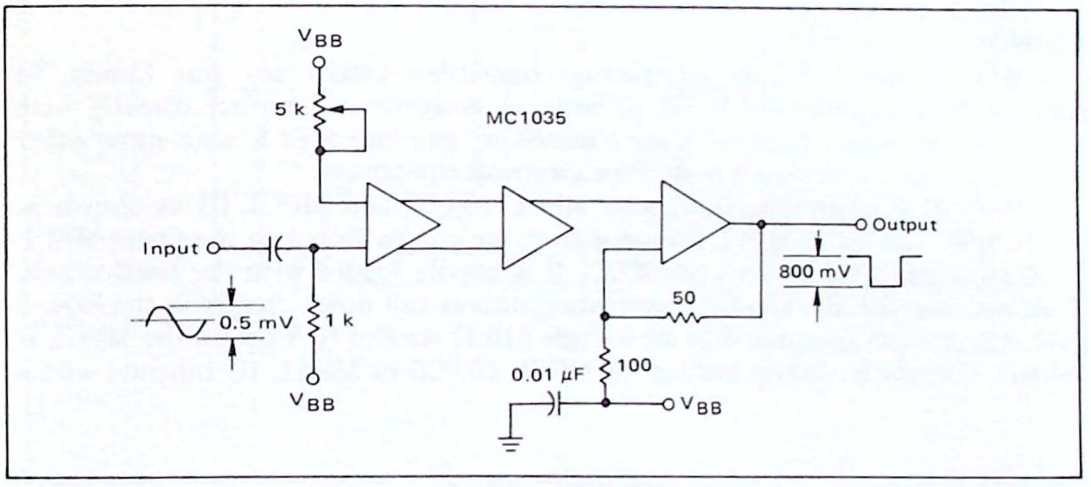


The retriggerable one shot multivibrator is useful for many applications, for example, to determine the presence or absence of pulse trains. A MECL III retriggerable one shot is shown in Figure 8-49. This circuit recognizes a pulse train having pulses spaced up to 550 ns apart. The minimum input pulse width is dependent on the repetition rate of the incoming signal. The 550 ns delay time is adjustable with the RC time constant (C_1, R_1).

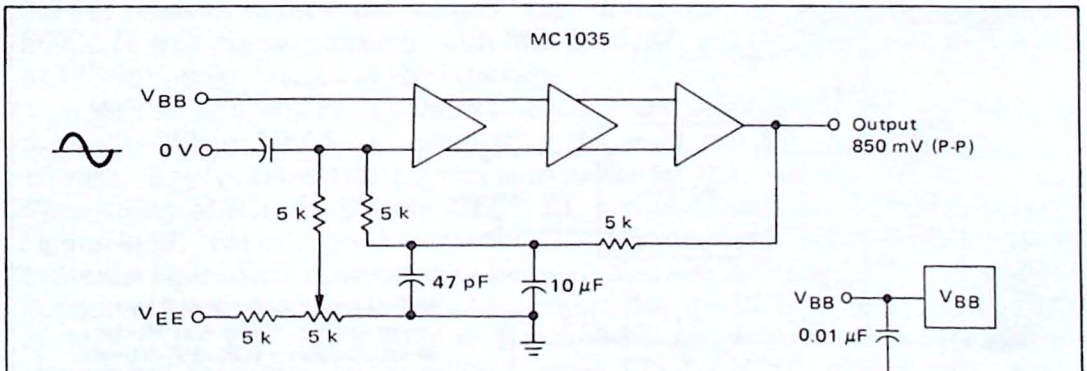
Linear Applications

The differential amplifier input of the basic MECL circuit allows the parts to be used in many linear applications. Some devices are made in all families with both inputs of the differential amplifier available outside the package. These MECL circuits are called Schmitt triggers or line receivers. Most circuits supply V_{BB} on an output pin for additional flexibility. Figure 8-50 and 8-51 illustrate two amplifiers

8-50: MECL II Amplifier/Schmitt Trigger



8-51: MECL II Video Amplifier



Voltage Gain = 600 V/V.
3 dB Down = 40 MHz @ Gain = 424 V/V.
Single-Ended Gain = 5.0 V/V Per Stage @ BW = 40 MHz.
Double-Ended Gain = 10.0 V/V Per Stage @ BW = 40 MHz.
Negative Feedback or Fewer Stages May Be Employed to Reduce Gain and Increase Bandwidth.

using the MC1035. The circuit in Figure 8-50 is useful for shaping and amplifying low level signals up to MECL signal levels. The Schmitt trigger third stage assures good edges. The bandwidth is about 40 MHz for the MC1035, but can be increased by using faster MECL circuits. The MECL 10,000 MC10115 has 10 dB of gain per stage at 100 MHz when used as an amplifier. The MECL III MC1692 is useful beyond 300 MHz, although care must be taken in circuit layout to avoid oscillation at these high frequencies.

Additional flexibility of MECL circuits is demonstrated by the MC1019 adder, used as a balanced modulator as shown in Figure 8-52. The three-level series gating required for this circuit is not available in the faster adders, but the speed of the MC1019 is adequate for many applications. When properly adjusted, carrier suppression is quite good.

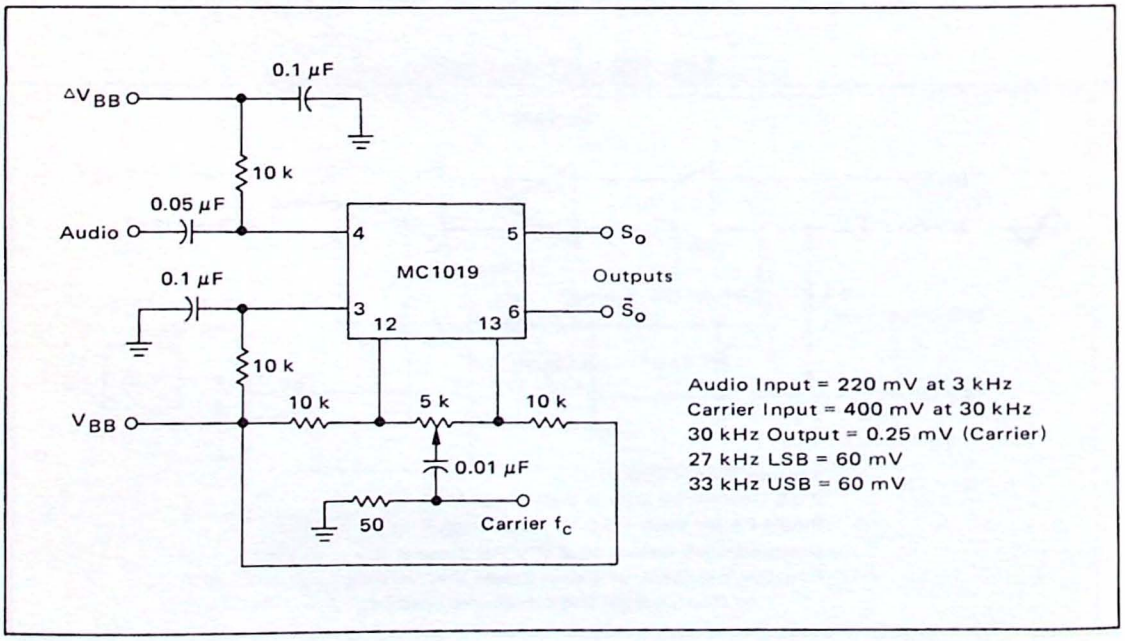
Introduction of the MECL MC1650 A/D comparator set a new standard for high speed A-to-D conversion. A 3-bit parallel A-to-D converter is shown in Figure 8-53. The MC1650 is limited to 6-bits conversion because of hysteresis in the circuit. The MC1650 is also used in serial conversions to save on parts – but with some sacrifice in speed.

Translators

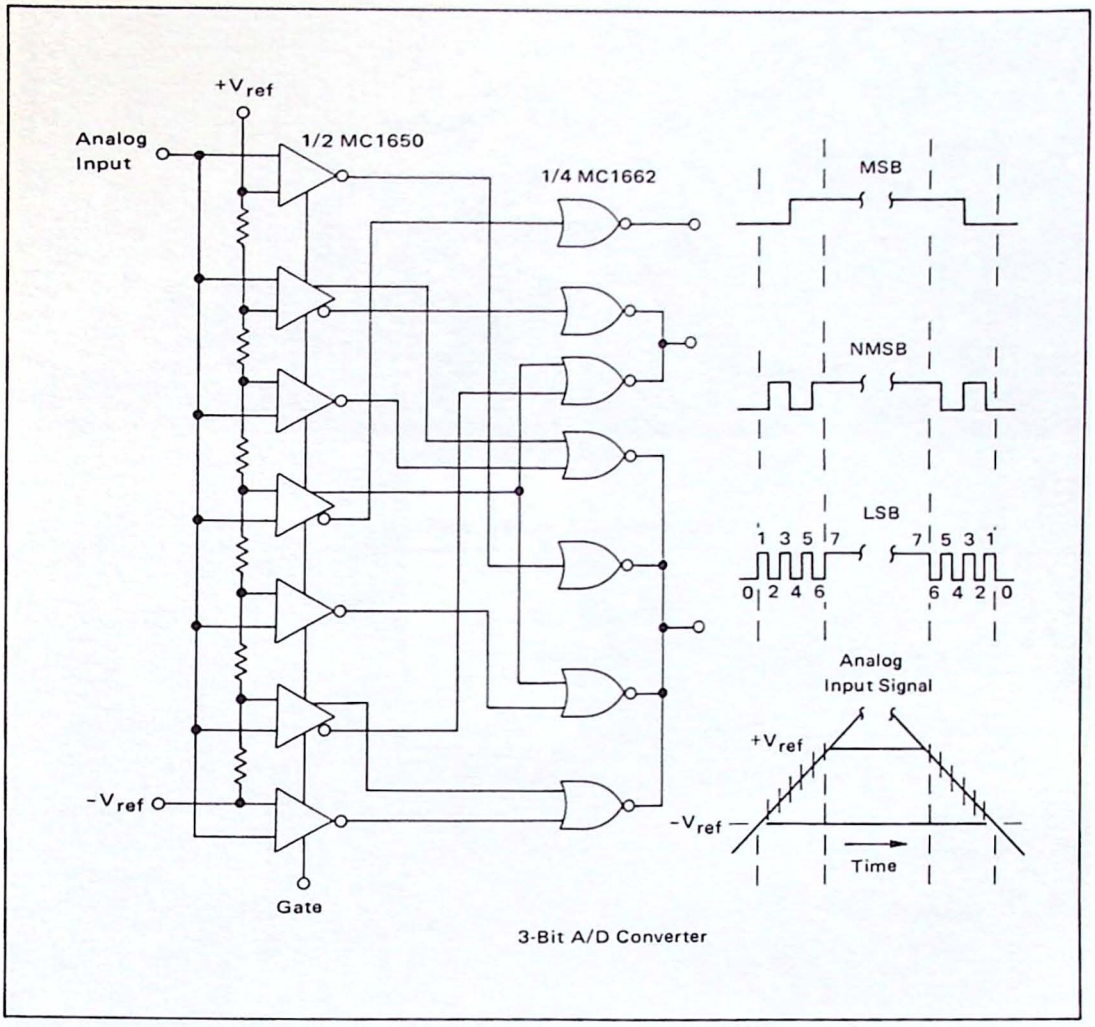
MECL signal levels are completely compatible within any one family. In addition, MECL 10,000 and MECL III parts are designed to interface directly with each other. However, translators are required to interface MECL with most other logic families and with signals from other electrical equipment.

MECL II is easily interfaced with MECL 10,000 and MECL III as shown in Figure 8-54. The higher MECL II output levels are compatible with the faster MECL 10,000 and MECL III inputs when MECL II is heavily loaded with the resistor pair. While not essential, the resistor combination insures full noise margin in the logic ∅ level. An alternate approach is to use a single 510 Ω resistor to V_{EE} on the MECL II output. Conversely, lightly loading the MECL 10,000 or MECL III outputs with a

8-52: MECL II Balanced Modulator



8-53: MECL III Analog-to-Digital Converter

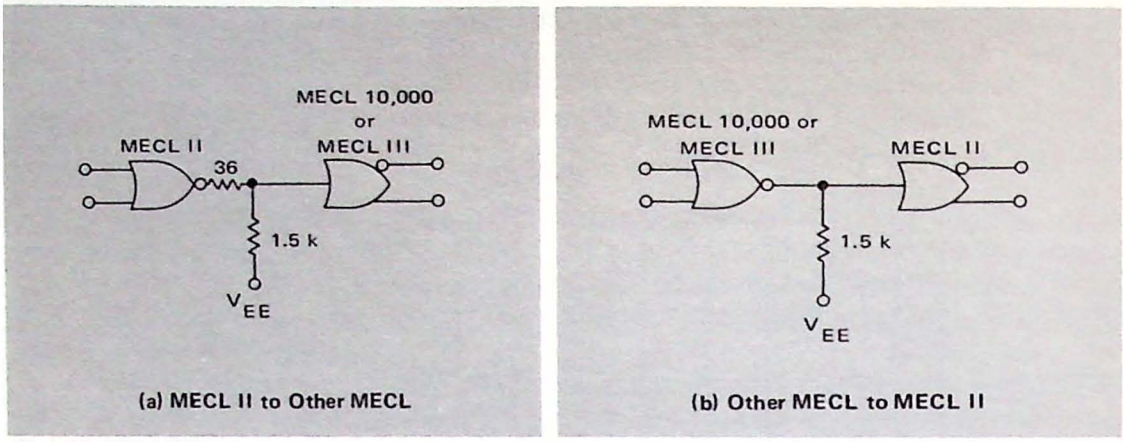


2.0 kΩ resistor raises the output logic levels to meet MECL II requirements. MECL II will operate directly with MECL 10,000 and MECL III, but there is a loss of 115 mV noise margin at the interface.

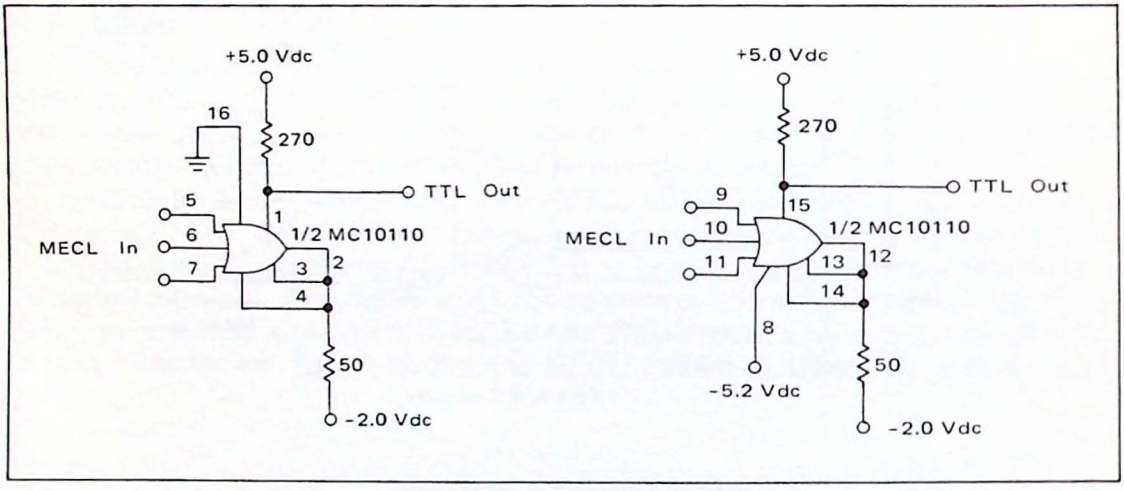
MECL and MTTL or MDTL circuits are interfaceable by any of several methods: When MECL is operated at the recommended -5.2 volts and TTL at +5 volts supply, translator circuits such as the MC1017 and MC1039 may be used. When using MECL 10,000 or MECL III, a circuit using the MC10110, shown in Figure 8-55, makes a good translator. If a -2 volt supply is not available, the two Thevenin equivalent resistors may be used as shown in Figure 3-25. The MC10110 has the advantage of being a dual translator, but the MC1026 or any MECL 10,000 or MECL III gate (as shown in Figure 8-56) may be used. The MC1650 A/D comparator is useful for very high speed TTL to MECL translation.

For many small systems it is not practical to have two supplies, with MECL operating at -5.2 volts and TTL at +5 volts. No integrated circuit translators are available for interfacing with both circuit types at +5 volts; however translation is easily accomplished with discrete components as shown in Figure 8-57. These circuits are fast enough for any available TTL.

8-54: Interfacing MECL II to MECL III or MECL 10,000



8-55: Dual MECL to TTL Interface

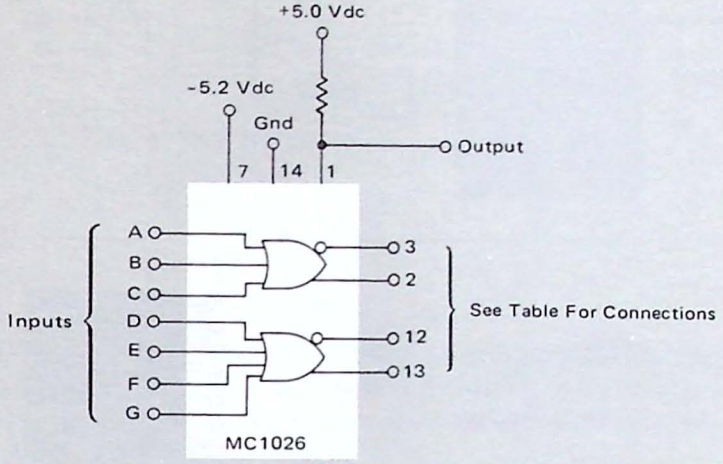


MECL also interfaces readily with MOS. With CMOS operating at +5 volts, any of the MECL to TTL translators works very well. On the other hand, CMOS will drive MECL directly when using a common supply. P-channel MOS, operating with a negative supply, requires simple translators as shown in Figure 8-58.

MECL translators such as the MC1018 are used with transistor buffers for lamp driving as shown in Figure 8-59. These circuits are also used for interfacing with most discrete component circuits when the input must drive the base of a grounded emitter transistor. The MECL to MOS translator circuit in Figure 8-58 drives a lamp connected to a negative voltage. These circuits can be further buffered for driving relays and other equipment with high current requirements.

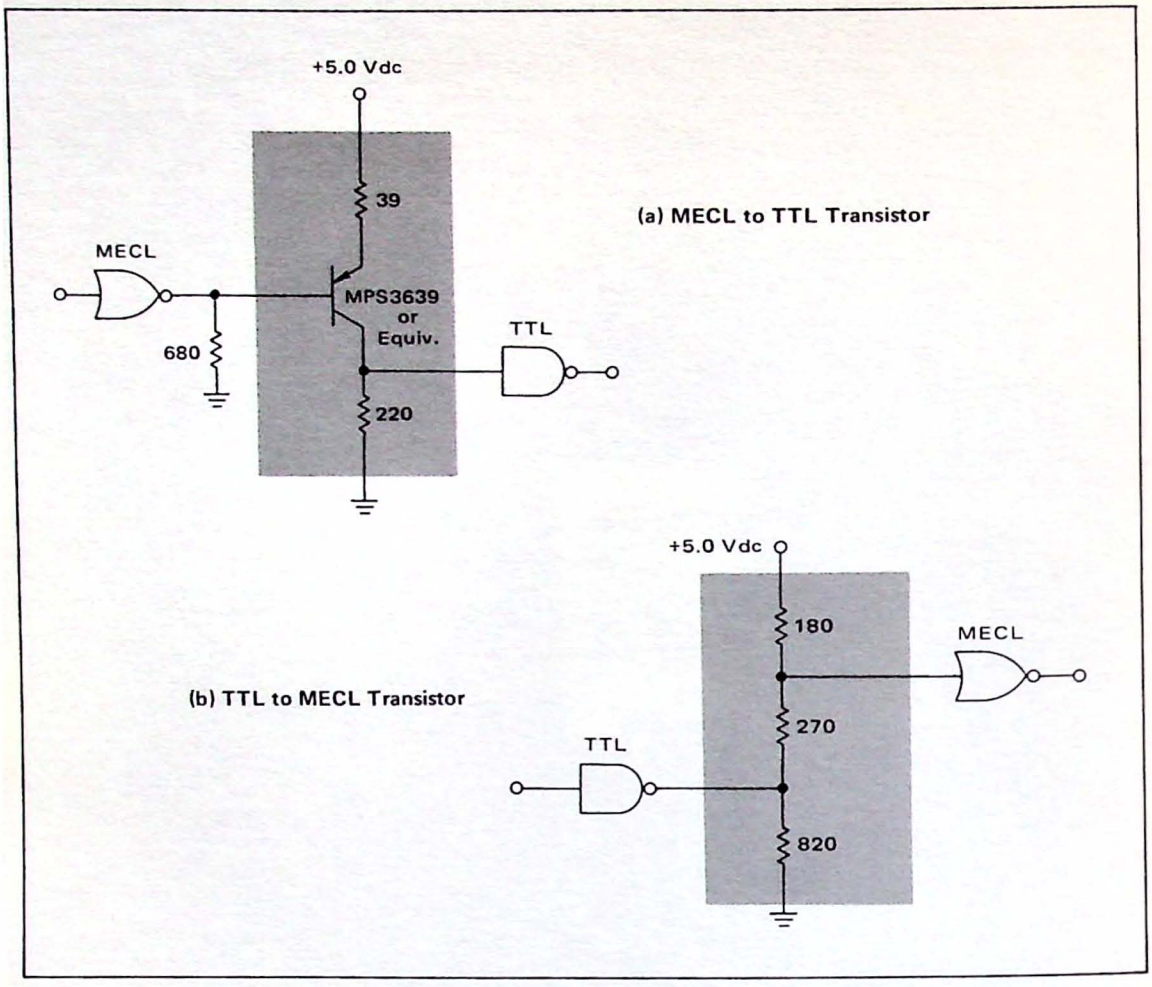
Important when designing indicator displays is the ability of MECL 10,000 and MECL III to drive light emitting diodes (LEDs) directly. The LED is connected between the MECL output and V_{CC}. The MECL 1 level is adequate to hold the diode off, and a $\emptyset$ level is sufficient to allow the diode to conduct. Current in the light emitting diode is controlled by the size of the pulldown resistor between the MECL output and V_{EE}.

8-56: High Speed MECL to Saturated Logic Translator

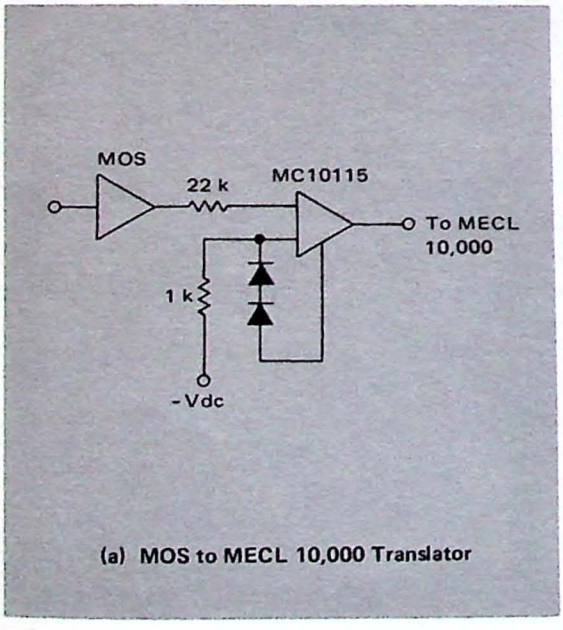


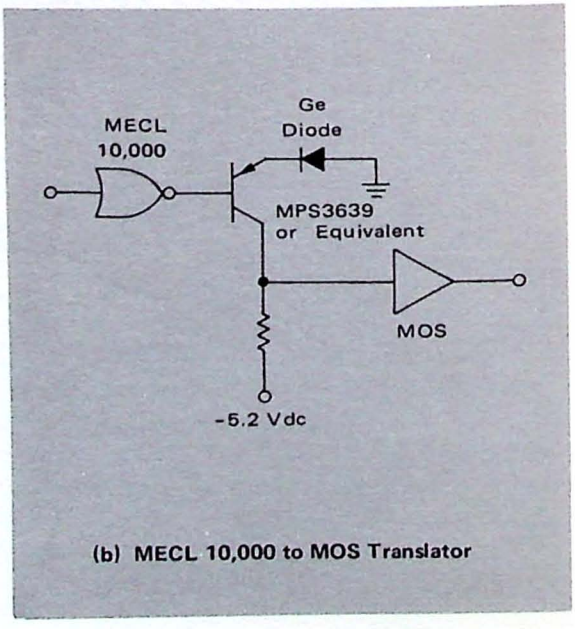
PIN	BIAS				OUTPUT
	3	2	12	13	
	-1.2 V	Open	-1.2 V	Open	(A + B + C) (D + E + F + G)
	-1.2 V	Open	Open	Open	A + B + C
	Open	-1.2 V	Open	-1.2 V	$\bar{A}\,\bar{B}\,\bar{C}\,\bar{D}\,\bar{E}\,\bar{F}\,\bar{G}$
	Open	-1.2 V	Open	Open	$\bar{A}\,\bar{B}\,\bar{C}$
	-1.2 V	Open	Open	-1.2 V	(A + B + C) $\bar{D}\,\bar{E}\,\bar{F}\,\bar{G}$

8-57: TTL/MECL Interfaced with Discrete Components, to Permit Common Supply Voltage Operation

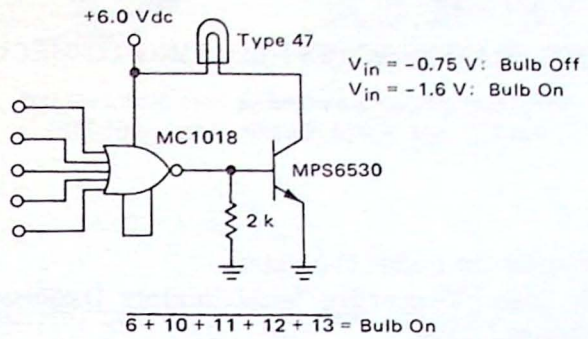


8-58: MECL 10,000/MOS Interface





8-59: MECL II Lamp Driver



The MECL line receiver and Schmitt trigger circuits are ideal for interfacing low frequency sine waves and low amplitude signals to MECL. An example of this type of circuit was shown in Figure 8-50 and described earlier in this chapter under the heading, "Linear Applications."

A CONCLUDING COMMENT

The wide variety of applications shown in this chapter illustrates the versatility of MECL integrated circuits. Although used primarily in high performance digital equipment, these circuits have been designed into all types of electronic equipment. The circuits exhibited in this section are intended as design ideas for using MECL, and are not meant to restrict the user to the particular applications shown.

Motorola has incorporated the features necessary for high system performance into MECL circuits. How well this performance is translated into an operating system is measured by the ingenuity and imagination of the System Designer.

APPLICATION NOTES RELATING TO MECL

(Application notes are available from Motorola Inc.
at P.O. Box 20924 Phoenix, Arizona 85036)

AN-417A	IC Crystal Controlled Oscillators
AN-418	High Speed Monostable Multivibrators Designed with MECL Integrated Circuits
AN-487	A High-Speed Ripple-Through Arithmetic Processor
AN-488	High-Speed Addition Using Lookahead Carry Techniques
AN-496A	Error Detection and Correction Using Exclusive-OR Gates and Parity Trees
AN-504	The MC1600 Series MECL III Gates
AN-532A	MTTL and MECL Avionics Digital Frequency Synthesizer
AN-534	Commutating Filter Techniques
AN-536	Micro-T Packaged Transistors for High Speed Logic Systems.
AN-553	A New Generation of Integrated Avionic Synthesizers
AN-556	Interconnection Techniques for Motorola's MECL 10,000 Series ECL
AN-565	Using Shift Registers as Pulse Delay Networks
AN-566	High Speed Binary Multiplication Using the MC10181
AN-567	MECL Positive and Negative Logic
AN-572	Initial Reliability Report for MECL 10,000 Integrated Logic Circuits
AN-573	Engineering Report: A Comparison Between MECL 10,000 and Schottky TTL Minicomputer Designs
AN-579	Testing MECL 10,000 Integrated Logic Circuits
AN-581	An MSI 500 MHz Frequency Counter Using MECL & MTTL
AN-583	A MECL 10,000 Main Frame Memory System Employing Dynamic MMOS RAMS
AN-584	Programmable Counters Using the MC10136 and MC10137 MECL 10,000 Universal Counters
AN-586	Measure Frequency and Propagation Delay with High Speed MECL Circuits

CHAPTER 9 MECL 10,000 AC Noise Immunity

Introduction

The noise margins of a logic family are very important to a system designer. A complete understanding of the circuits' ability to reject noise allows the user to design a power distribution network and circuit boards compatible with the circuit requirements. Worst case noise margins are specified on the MECL data sheets and are discussed in the earlier chapters of this book. The dc noise margins are 125 mV for a HIGH output level and 155 mV for a LOW output level when using the MECL 10,000 family.

When designing "worst case" these dc values are used for calculating noise margin losses due to static system conditions. Included are power supply distribution losses as described in Chapter 5, and losses due to thermal differences as described in Chapter 6.

While a worst case design suggests the use of noise margins when considering transient effects such as crosstalk and ringing due to non-terminated signal lines, the dc noise margin values may be unnecessarily restrictive. MECL circuits have a response time to transients which can be used to ease the design rules for this type of noise.

Because of the large number of circuit types in the MECL product lines, this chapter of the MECL System Design Handbook will not characterize all parts. Worst case noise immunity is not specified on data sheets so any test results discussed here are typical, rather than worst case.

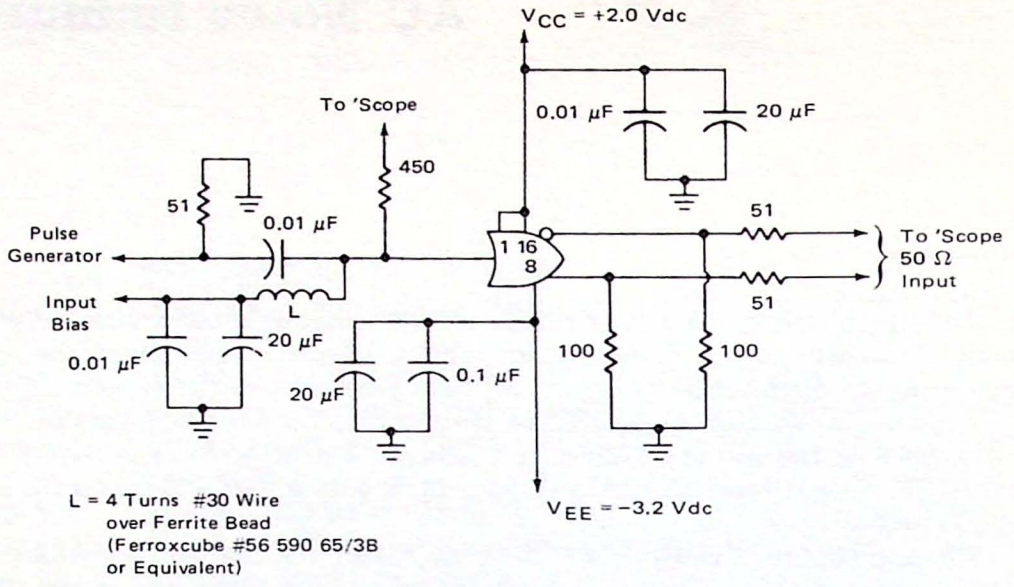
This chapter describes test circuits used to evaluate MECL 10,000 circuits for noise immunity, shows the test results, and discusses the variables in obtaining the test results. Anyone interested in measuring this type of data for other MECL parts is encouraged to build similar test fixtures and perform the tests to selected limits.

Test Circuits

Transient noise can enter a MECL circuit at one or more of four different points. These are: at the input to a circuit; on V_{CC}, which is normally ground; on V_{EE}, which is normally -5.2 Vdc; and on the termination voltage, V_{TT}, which is normally -2.0 Vdc. The response of the MECL circuit to noise depends on where the noise enters. For this reason separate tests are used to measure the response of a circuit to induced noise.

A test circuit for measuring noise immunity to a transient signal on an input line is shown in Figure 9-1. As is characteristic of MECL testing, the text fixture puts +2.0 V on V_{CC} and -3.2 V on V_{EE}, to permit terminating the MECL outputs to ground through a 50 Ω 'scope probe. This has proven to be the most accurate method for testing MECL 10,000 and MECL III because possible problems with high impedance 'scope probes are eliminated.

9-1: Input Noise Test Circuit



Both V_{CC} and V_{EE} are capacitor bypassed to ground to eliminate noise at these points. If the oscilloscope's 50-ohm input will handle the HIGH logic level (about +1.1 volts) accurately, the MECL circuit outputs may be connected directly to the oscilloscope inputs. If not, 2:1 attenuation resistors and 100-ohm pulldown resistors may be used as shown in the figure.

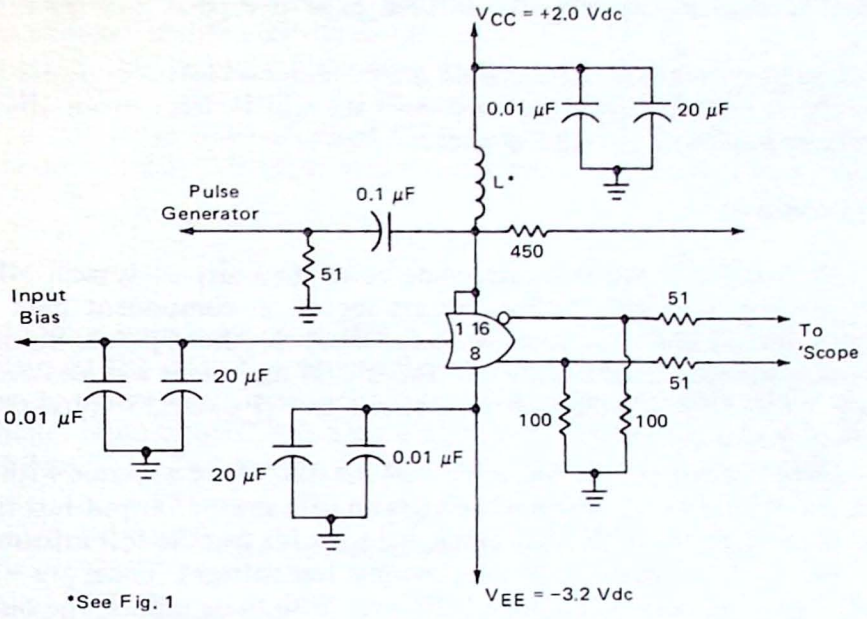
The input of the test circuit is arranged to utilize an accurate bias, provided by a power supply, to set the input logic levels. The pulse generator is terminated by a 51-ohm resistor and is capacitor-coupled to the input pin, to induce a noise pulse. An inductor, made of four turns of wire wound around a ferrite bead, isolates the noise from the input-bias source.

A 450-ohm resistor is used in series with the 50-ohm 'scope input to isolate the input from the 'scope. This results in a 10:1 amplitude attentuation, but still gives an accurate picture of the input noise.

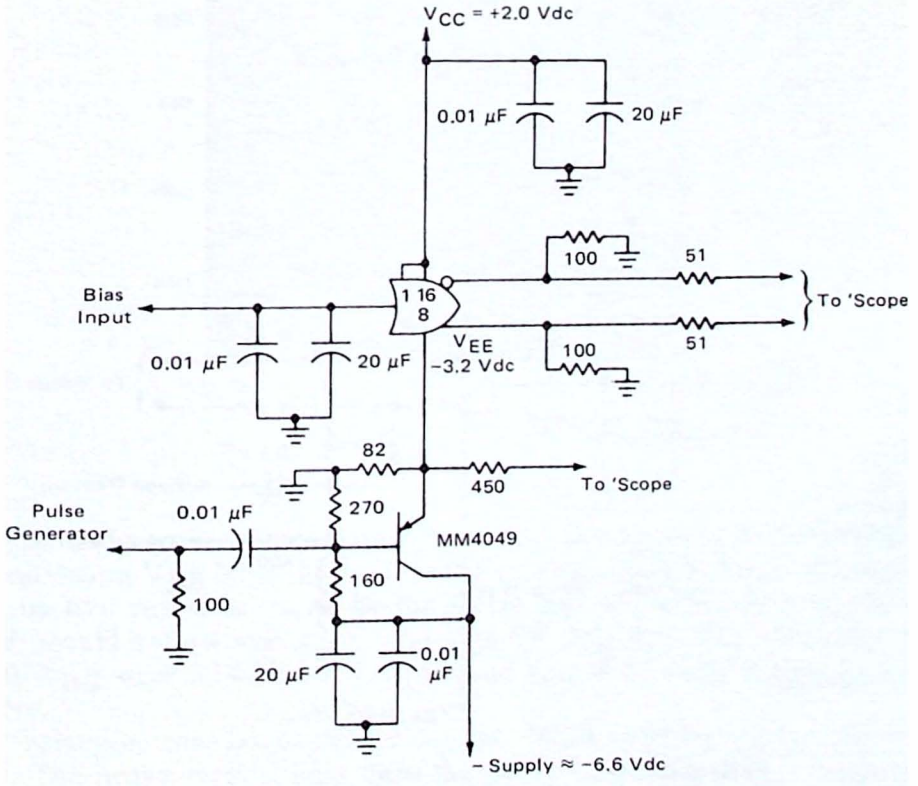
The response of MECL circuits to noise on the V_{CC} line is tested in a manner similar to that for input noise. A test circuit for V_{CC} noise is shown in Figure 9-2. A power supply is again connected to the circuit input to set the HIGH and LOW logic levels. The pulse insertion network is connected to V_{CC} pins 1 and 16. Since good MECL design practice is to tie both V_{CC} pins to a common ground, tests were not conducted for signals inserted on only one V_{CC} pin.

A slightly more complicated test circuit, Figure 9-3, was used to measure response to noise on V_{EE}. A PNP transistor is connected as an emitter-follower to provide a low-impedance V_{EE} path. The high speed pulse generator is capacitor-coupled into the base of the transistor. Because of the large signals required on V_{EE} to affect the circuit outputs, the emitter-follower transistor is used to allow better termination of the pulse generator than can be done with a resistor alone. V_{EE} noise amplitude is approximately equal to the maximum pulse output of the pulse generator used. A very high speed MM4049 transistor or equivalent should be used to retain the fast pulse edge speed.

9-2: V_{CC} Noise Test Circuit



9-3: V_{EE} Noise Test Circuit



Noise Immunity Test Conditions

V_{TT} noise tests were made with the circuit shown in Figure 9-4. Power supplies are connected to V_{CC}, V_{EE}, and the circuit input. Bypass capacitors are used to keep noise from these points. The output of the test circuit is arranged to insert noise on V_{TT}. For this test, the 51-ohm termination resistors are connected to ground through an inductor. The induced pulse is capacitor-coupled to the V_{TT} point.

Circuit outputs are isolated from the 50-ohm oscilloscope inputs by 450-ohm attenuation resistors. These resistors prevent the MECL circuit from driving both the 51-ohm resistors to V_{TT}, and the 50-ohm 'scope input.

Test Conditions

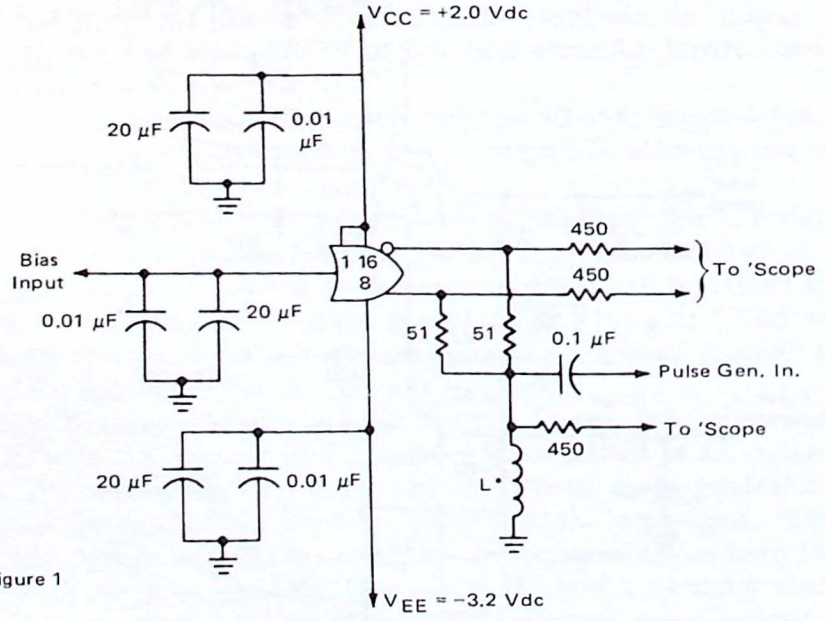
The test limits chosen to determine noise immunity of typical MECL 10,000 parts are based on the specified voltages shown on component data sheets. The circuit output was allowed to move to the input threshold points before the noise amplitude was considered a maximum. The HIGH* logic level was allowed to drop to V_{IHA}, 0.895 volts, and the LOW level to rise to V_{ILA}, 0.525 volts, (voltage given for V_{CC} at +2.0 V).

These two points were chosen because the outputs of a circuit with these input levels are defined by the threshold voltages on data sheets. Output test limits should be determined by the tester when evaluating parts for specific test information.

The input bias points were set at normal test voltages. These are +1.11 V for a HIGH logic level and +0.31 V for a LOW level. With these inputs, the outputs of the circuits under test averaged the following levels: V_{OH} "OR" = 1.100 V; V_{OH} "NOR" = 1.099 V; V_{OL} "OR" = 0.290 V; and V_{OL} "NOR" = 0.265 V.

Using the limits described above the following transitions were allowed on the outputs before maximum noise was reached: ΔV_{OH} "OR" = 0.205 V; ΔV_{OH} "NOR" = 0.204 V; ΔV_{OL} "OR" = 0.235 V; and ΔV_{OL} "NOR" = 0.260 V. This

9-4: V_{TT} Noise Test Circuit



* HIGH ≡ 1; LOW ≡ Ø.

technique for reading output transition amplitudes is used because it is more convenient than reading dc voltages on an oscilloscope.

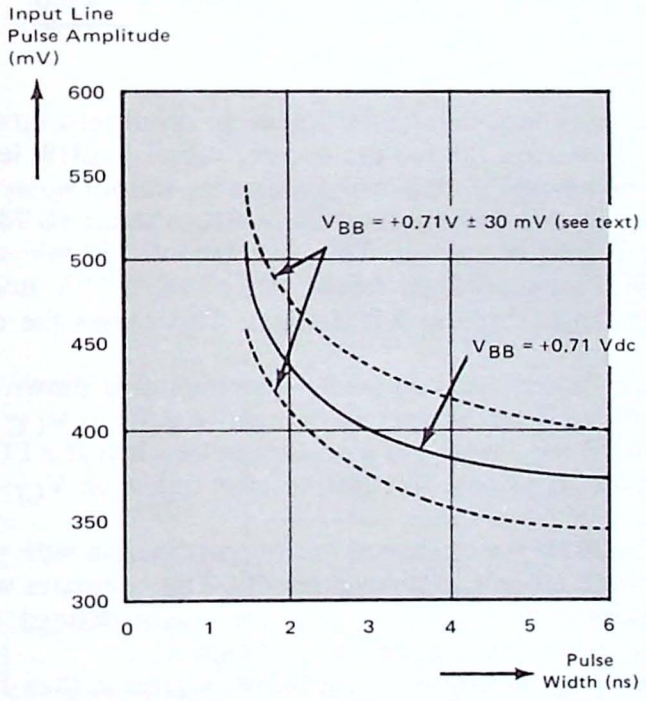
The tests are conducted by setting the power supplies and circuit inputs into the quiescient conditions. A pulse width is selected. Then the amplitude of the pulse generator is increased until the output reaches the predetermined limit. The pulse width is then changed and the test repeated.

To generate the narrow pulses used in the tests, a very high speed pulse generator (EH 129 or equivalent) was used. This generator is capable of 500 MHz operation and has pulse edges of about 0.5 ns rise time. This represents worst-case noise conditions, because this edge speed is much faster than would be expected in a MECL system.

Test Results

Typical noise immunity for a MECL 10,000 gate is shown in Figure 9-5. A pulse is applied to the circuit input and the pulse amplitude and width is measured to determine the tolerance limits previously defined. The average is shown by the solid line which levels at about 370 mV for a 6 ns pulse width. The curve is relatively flat to about 3 ns, then rises sharply as the circuit becomes bandwidth-limited.

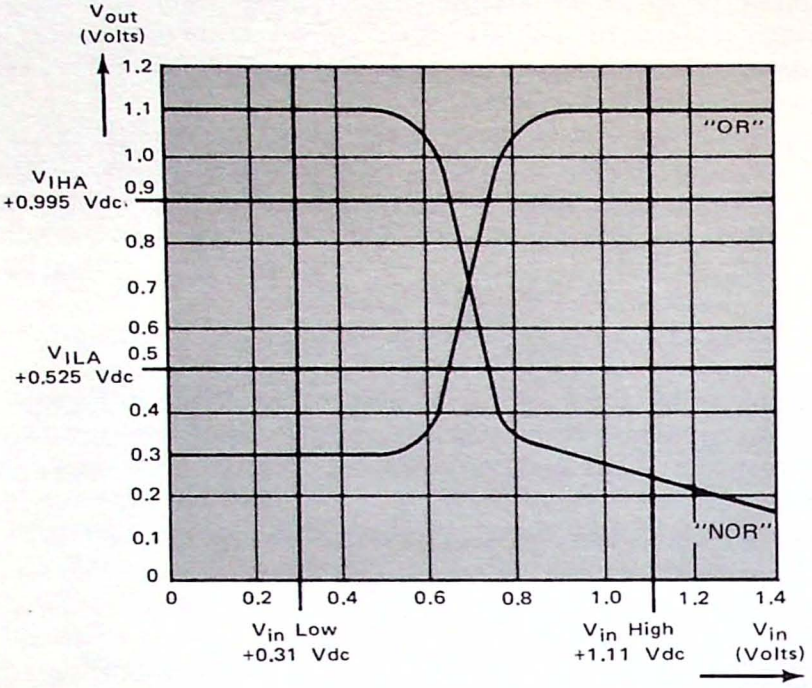
9-5: Input Signal ac Noise Immunity



Test results have shown that there is some deviation from the single line shown, due to variations in V_{BB} from the exact center voltage of 0.71 V. When this happens there will be two curves as shown by the dotted lines in Figure 9-5. V_{OH} OR and V_{OL} NOR would follow one curve, and V_{OL} OR and V_{OH} NOR the other. For example, if V_{BB} were 30 mV low, V_{OH} OR and V_{OL} NOR would follow the upper dotted curve.

This behavior can be explained by the MECL transfer curves shown in Figure 9-6. The heavy vertical lines show the nominal input test levels. The outputs

9-6: MECL 10,000 Transfer Characteristics



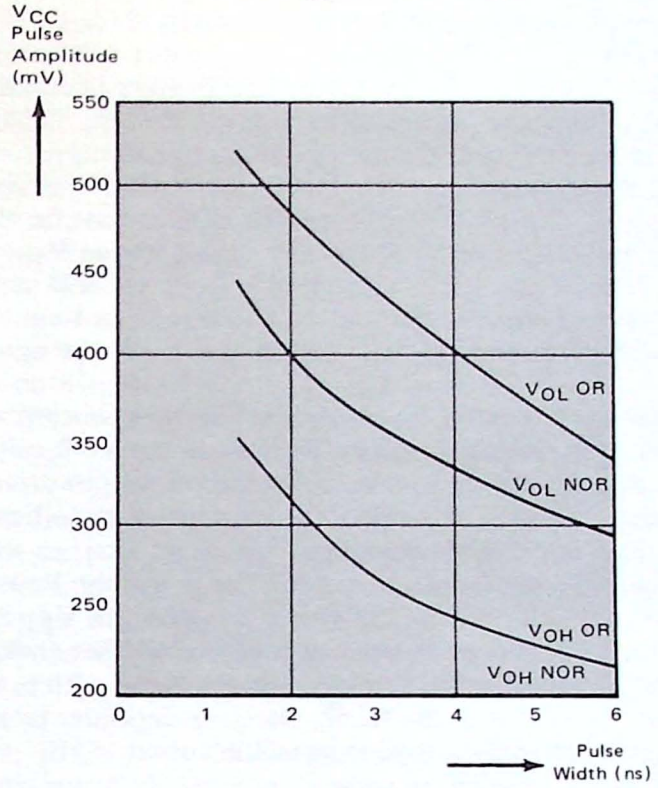
must move to the heavy horizontal lines. Under dc conditions (greater than about 6 ns pulse width), the circuit follows the transfer curve. A LOW level input has to move from +0.31 volts to about +0.67 volts before the output noise limit is reached. Similarly, a HIGH input has to move from 1.11 volts to about +0.74 volts before the maximum output change is reached. This gives about 370 mV noise margin, as shown in Figure 5. If V_{BB} is slightly to one side of the 0.71 V nominal value, the transfer curves shift slightly to the left or right. This causes the dotted curves of Figure 9-5.

Noise immunity to transients on the V_{CC} supply line is shown by the curves in Figure 9-7. The tests are made by applying a negative pulse to V_{CC} when the tested outputs are at a HIGH logic level, and a positive pulse when at a LOW level output. The circuits are most susceptible to negative noise spikes on V_{CC} – affecting the HIGH logic levels.

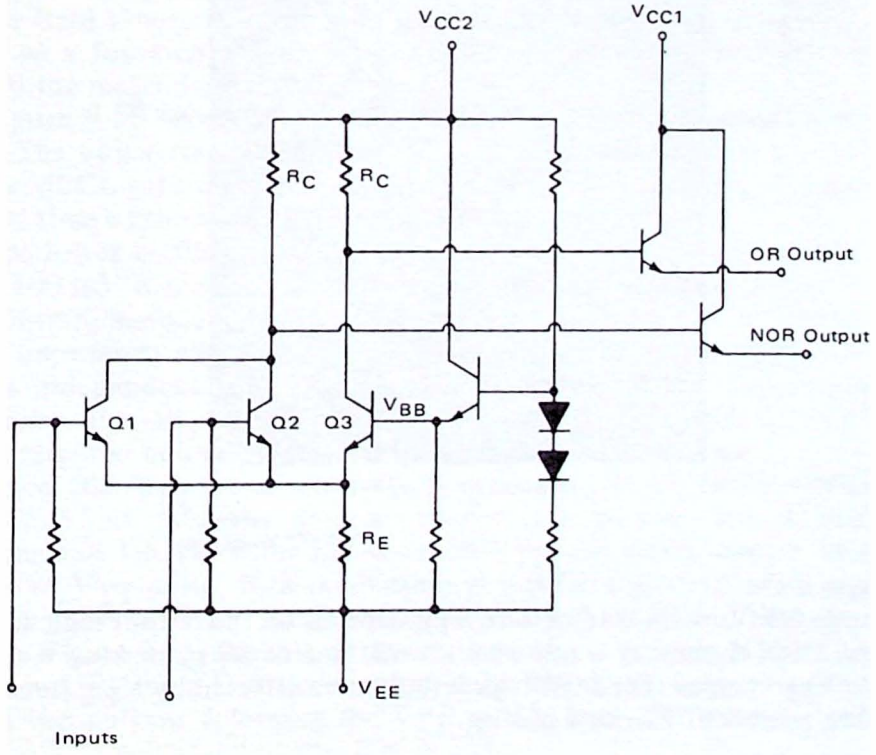
For wide pulses there is a one-to-one loss of noise margin with pulse amplitude. At 6 ns, there is about 215 mV of noise immunity. This compares with the 204 mV maximum output transient allowed by the previously defined test limits. For narrower pulses the response time is shown in the figure.

The noise immunity to positive-going pulses is greater than for the negative-going transient in a MECL gate. This can best be explained by the gate schematic shown in Figure 9-8. A positive going pulse on the V_{CC} lines increase the total voltage across the circuit. With the output at a LOW logic level, the change in output level to V_{CC} is due to the ratio of R_C to R_E, and to the voltage drop across the switch transistor. In a MECL gate the LOW output will follow V_{CC} at about a 3 to 4 amplitude ratio, i.e., V_{CC} noise is attentuated about 25%. As a result, the degree of coupling of noise on V_{CC} to the outputs is dependent on the output logic level rather than on the direction of the noise signal. However, since HIGH level noise margin is only reduced by a negative signal on V_{CC}, the circuit is more vulnerable to negative going transients than positive ones.

9-7: V_{CC} ac Noise Immunity



9-8: MECL Gate Schematic



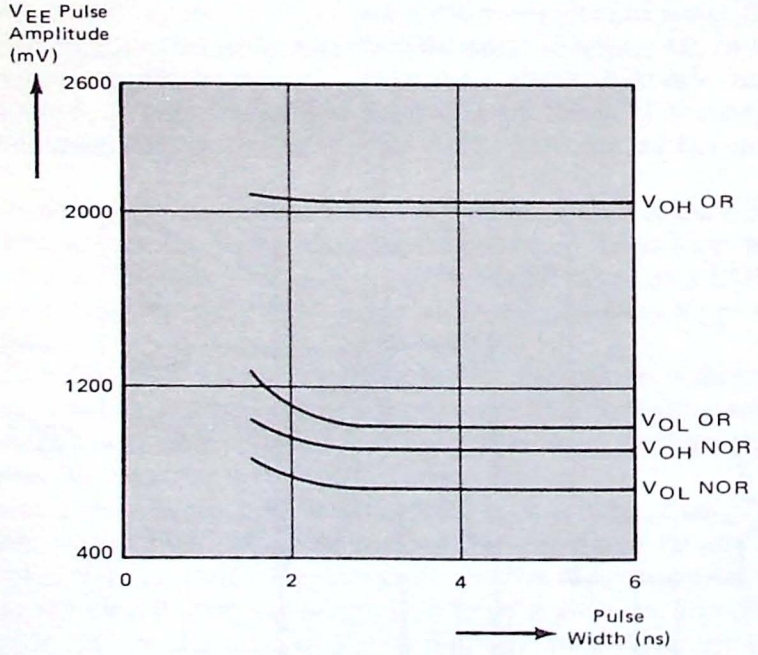
The V_{CC} noise margin is approximately the same for the HIGH level OR and NOR outputs. However, the OR and NOR noise immunity differs when the outputs are at a LOW logic level. This is again explained by the gate schematic of Figure 9-8. With both inputs LOW, Q_1 and Q_2 are turned off and Q_3 is conducting. With a positive pulse on V_{CC}, V_{BB} goes more positive, insuring that Q_1 and Q_2 remain off. There is no tendency for the gate to change logic states.

However, when one or both of the inputs are HIGH, the current path is through the Q_1 Q_2 pair, giving a LOW level on the NOR output. In this case, when V_{BB} rises due to a positive spike on V_{CC}, the difference between V_{BB} and the input signals is reduced. If the noise spike is sufficiently large, Q_3 will start conducting some of the switch current. This in turn causes the NOR output to go more positive. For a positive pulse on V_{CC}, the V_{BB} bias voltage will track the signal with about 85% amplitude.

Another reason for less noise immunity on the NOR output is due to the collector resistors R_C. The collector resistor connected to the NOR output transistor has a smaller value than the resistor connected to the OR output driver (220 ohms, compared to 245 ohms, typical). This makes the noise attenuation less for the NOR output by the difference in the R_C to R_E ratios.

The noise immunity to transients on the V_{EE} supply line is shown in Figure 9-9. The tests are performed by applying a pulse on the V_{EE} line, using the circuit shown in Figure 9-3. The pulse polarity is chosen so that there is a positive pulse on V_{EE} when the output is LOW, and a negative pulse with a HIGH output. The amount of noise immunity in the MECL circuit is dependent on whether the OR or NOR output is tested, and the logic state of the output.

9-9: V_{EE} ac Noise Immunity



The rate MECL outputs track with V_{EE} depends on the output logic level. The HIGH logic state changes at a rate about 1.6% that of V_{EE}, making it relatively immune to V_{EE} changes. The LOW logic level is more affected by V_{EE} fluctuations, changing at a rate about 25% that of V_{EE}.

V_{BB} changes at about 15% of V_{EE}. This is not sufficient to shift the transfer curves enough to affect output levels. However, because of the very fast rise and fall times (0.5 ns) of the pulse generator used in these tests, there is some capacitive coupling between V_{EE} and V_{BB}.

Referring to the schematic in Figure 9-8 it can be observed that the noise coupling into V_{BB} is seen primarily on the NOR output. Coupling on V_{BB} is toward the input logic level when measuring NOR output noise immunity, and away from the input level when testing to OR outputs.

Example: when testing the NOR output with inputs LOW, the output is HIGH and a negative pulse is applied to V_{EE}. This negative pulse couples into V_{BB} and causes it to move toward the LOW level inputs. If the V_{EE} noise is sufficiently large, both halves of the logic switch will start conducting and the output will move toward the opposite logic state. This gate switching will also be seen on the OR output, but since the V_{EE} pulse is opposite in polarity to the OR output movement, coupling of V_{EE} to the output offsets the effects of V_{BB} transients. Normally, about 2 volts of noise immunity exists for the OR output in this test condition.

From Figure 9-9 it may be seen that the OR outputs have more noise immunity than the NOR outputs (as would be expected from the V_{BB} coupling). HIGH logic levels are more immune than LOW levels due to the voltage tracking ratio of the output logic levels with V_{EE}.

The LOW level NOR output is most affected by V_{EE} noise. This is due to a combination of V_{OL} tracking and V_{BB} coupling. However, the noise immunity to this worse case condition remains greater than 700 mV. The greatest immunity occurs on the HIGH level OR output and is greater than 2 volts. In general, the MECL circuits are more immune to noise on V_{EE} than on any other point in the system.

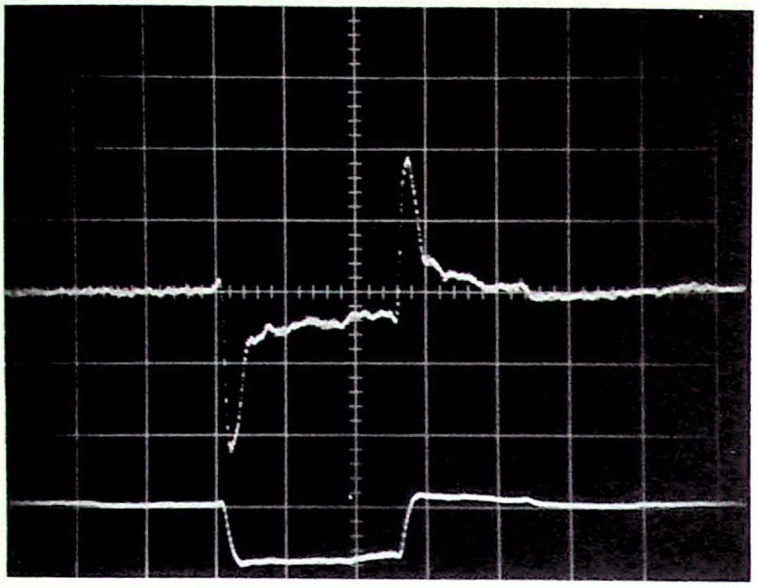
The noise immunity of MECL circuits to noise on the V_{TT} termination voltage is dependent on the output impedance of the MECL gate and on the response time of the MECL circuit. The test circuit in Figure 9-4 shows that the pulse generator signal is connected to the outputs through 50-ohm termination resistors. Since the resistors have a better bandwidth than the pulse signal, there is no noise immunity change as a function of pulse width. Full amplitude output transitions are present down to the measuring limit of about 1.5 ns.

Figure 9-10 shows waveforms associated with V_{TT} noise immunity measurements. The upper trace shows the noise pulse coupling through to the circuit output and the MECL gate recovering from the pulse and then restoring the logic level. The response time of the MECL 10,000 output circuit is about 2 ns.

The lower oscilloscope trace shows the pulse generator noise on the V_{TT} line. About 400 mV is required to cause a 204 mV transient on the output. The ratio of noise amplitude on the V_{TT} line to the noise on the output is dependent on the output impedance of the MECL circuit. As a result, the noise immunity to fast pulse edges is independent of the OR or NOR output tested and of the polarity of the noise pulse. For all outputs, about 400 mV of V_{TT} noise with 0.5 ns rise and fall times is required before the test limits are reached.

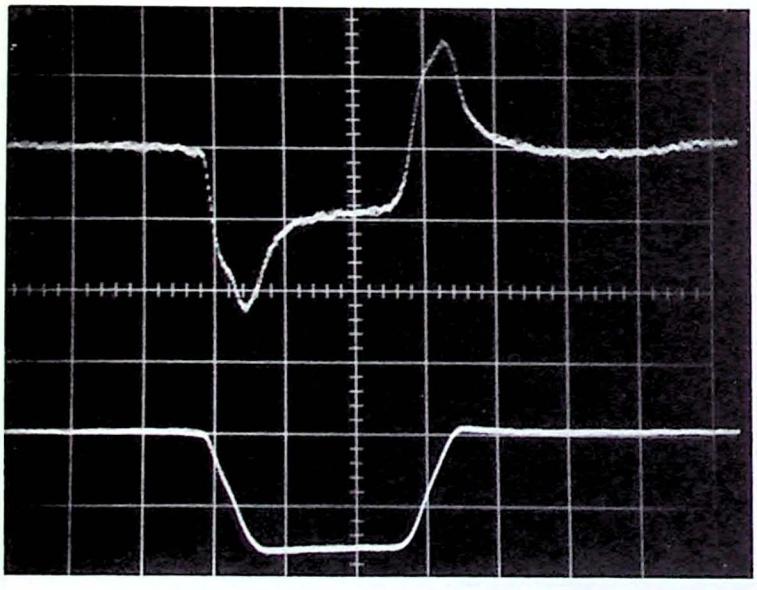
Since the V_{TT} noise immunity is dependent on the MECL circuit response time, the 0.5 ns pulse rise times are a worst case test condition. By increasing the pulse rise and fall times for the noise on V_{TT}, the MECL circuits become more immune to V_{TT} noise. With the outputs at a HIGH logic level and a negative pulse with 2 ns edges on V_{TT}, the MECL circuits have about 800 mV noise immunity, as shown in Figure 9-11. Because of the emitter-follower outputs of MECL circuits, the noise immunity for a LOW level output is limited by the output transistors turning off and the outputs following the V_{TT} voltage level. For example, with V_{TT} at

9-10: V_{TT} ac Noise Immunity With 0.5 ns Noise Edge Speed



Horizontal scale = 5.0 ns/cm

9-11: V_{TT} ac Noise Immunity With 2 ns Noise Edge Speed



Horizontal scale = 5.0 ns/cm

ground in the test circuit, and a low level noise margin output test limit of 0.525 volts, the maximum tolerable positive pulse amplitude on V_{TT} is 525 mV.

Conclusions

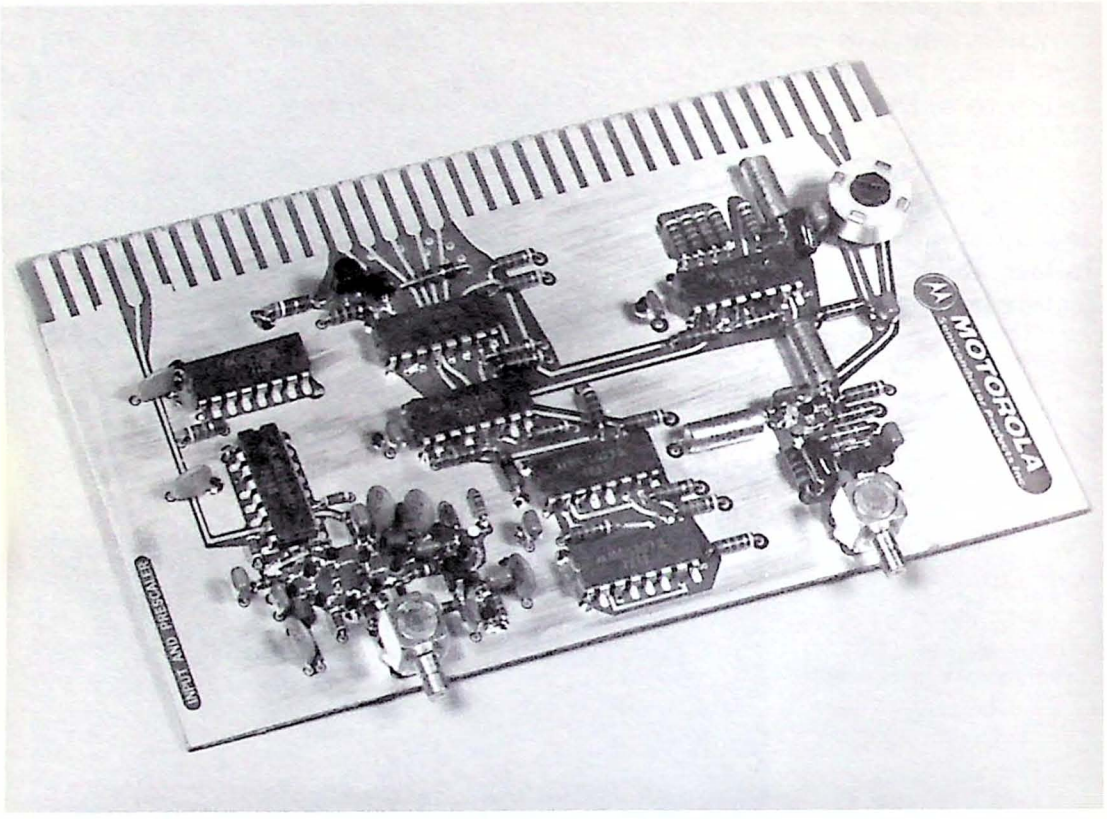
The MECL circuits are most susceptible to noise on the V_{CC} supply line. For this reason, MECL design rules commonly suggest operating MECL circuits with a

positive ground on V_{CC} and -5.2 volts on V_{EE}. By having a low impedance system ground, noise on the V_{CC} line between two circuits can be controlled and minimized.

In some cases it is desirable to operate MECL circuits with ground and +5 volt supplies. MECL circuits operate very well in this mode when care has been taken to keep noise on the +5 volt supply line to a minimum. The MECL circuits are most immune to noise on the V_{EE} supply line. With standard capacitor bypassing techniques, noise on the V_{EE} line is controlled to safe system levels.

The amount of noise present in a digital system is dependent on many factors – such as power supplies and system environment. A primary source of noise is crosstalk, which is proportional to signal speed and signal amplitude. The 800 mV logic swing and relatively slow rise and fall times of MECL 10,000, along with its ability to operate in a transmission line environment, serve to reduce crosstalk in a MECL system.

One factor contributing to power supply noise is the amount of current "spiking" inherent in a logic family. MECL circuits have emitter-follower outputs and differential-amplifier switches. Consequently MECL generates very little noise. In fact, the high ratio of noise immunity, to internally generated noise in MECL, is a feature leading to reliable system operation.



Shown here are two prescalers for a frequency counter. At left is a 500 MHz prescaler employing the MC1690 flip-flop and the MC1678 (both MECL III devices). The rest of the board contains a 150/200 MHz prescaler and control, built with MECL 10,000 circuits. Input amplifiers are included on the board for each prescaler. Scaled-down frequency outputs ($\leq$ 35 MHz) are fed into a low speed counter.

CHAPTER 10 MECL 10,000 For Military Applications

To achieve state-of-the-art logic systems for military applications, a logic family is needed with MECL speed and system benefits, and this logic family must operate over the −55°C to +125°C military temperature range (MIL-TEMP).

MECL II has been available for a number of years with the MIL-TEMP rating and many military systems have been designed with this logic series. However, discussion in this chapter will be limited to the MIL-TEMP version of MECL 10,000 – the MC10500 and MC10600 Series. The reason is that these devices are most applicable for new designs. The chapter will examine system design rules as they apply to MIL-TEMP MECL 10,000 Series parts.

The primary system difference between the MECL 10,000 MIL-TEMP part types and the commercial range MECL 10,000 parts, is that MIL-TEMP parts are specified to drive 100-ohm (min) loads instead of 50-ohms (min). The MECL 10,000 MIL-TEMP Series part types are of the same logic configurations and power dissipation levels as their commercial temperature range equivalents. To obtain the military temperature range equivalent of a commercial temperature range part type, add 400 to the commercial temperature range part (i.e., MC10109 MIL-TEMP equivalent is MC10509).

In order to achieve the high speeds of MECL 10,000, capacitances an inductances on the IC chip must be held to a minimum. Thus, geometries of th bipolar devices used in the logic functions are small. Small geometry devices are n compatible with high output-current drive requirements (50-ohm load to −2.0 V, a with commercial temperature range MECL 10,000) in a high temperature environment (+125°C). Consequently MIL-TEMP MECL 10,000 logic functions are specified with 100 ohms (min) line driving capability.

MIL-TEMP MECL 10,000 operation at +125°C will be highly reliable if the system designer follows the guidelines given in this chapter. Most systems, even those operating in the commercial temperature range, use a 100-ohm transmission line environment. Therefore the restriction will not inhibit system design.

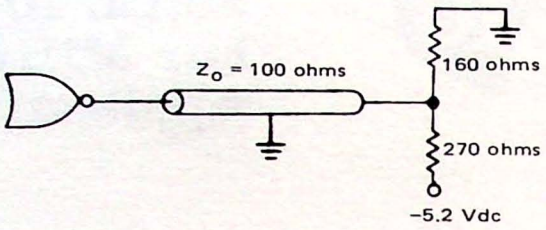
Fanout

For good AC performance, fanout should be limited to 10. For further details and wire rules regarding permissible maximum line lengths for given fanout levels, refer to Chapter 3.

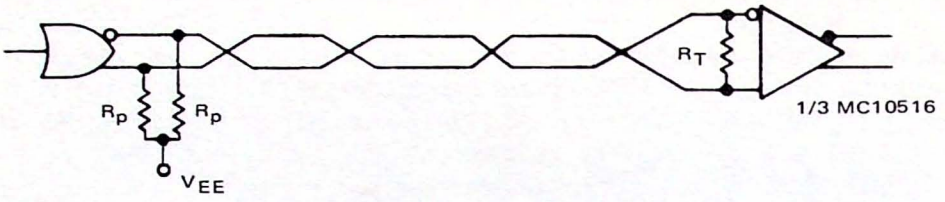
Termination and Interconnect Techniques

For a transmission line environment, 100 ohms is the minimum value of parallel termination resistance recommended. A parallel termination may be achieved by using a single 100-ohm resistor to −2 Vdc, or by using a Thevenin equivalent termination as shown in Figure 10-1.

For unterminated or series terminated interconnects, a 510-ohm resistor to V_{EE} will provide the proper current path for the output devices of the driving gate. Values between 510 ohms and 2 k ohms may be used. For further details, see Chapters 3 and 5.



10-1: Thevenin Equivalent Termination Technique



10-2: Twisted Pair Termination to V_{EE}

Wiring rules for the layout of printed circuit boards and other interconnect techniques will follow the guidelines given in Chapters 3 and 4 for the standard MECL 10,000 series.

Twisted pair may be used with the MECL 10,000 MIL-TEMP parts. One termination technique recommended for this type of cable is shown in Figure 10-2.

In Figure 10-2 the values of the resistors R_P may be any value from 510 ohms to 2 k ohms. R_T will be the same as the characteristic impedance of the line, Zo, ($R_T \geqslant 100$ ohms).

Power

Computations of system power dissipation can be accomplished by referring to Chapter 5 and Table 5-3.

Noise Margin

As stated in Chapter 4, noise margin is defined as the difference between a worst case input logic level and the worst case output threshold level closest to that logic level. Guaranteed noise margin (N.M.) for the MECL 10,000 MIL-TEMP series is:

$$NM_{1\ level} = V_{OHA\ min} - V_{IHA\ min}$$

$$= -0.950\ V - (-1.105V) = 155\ mV;$$

$$NM_{\emptyset\ level} = V_{ILA\ max} - V_{OLA\ max}$$

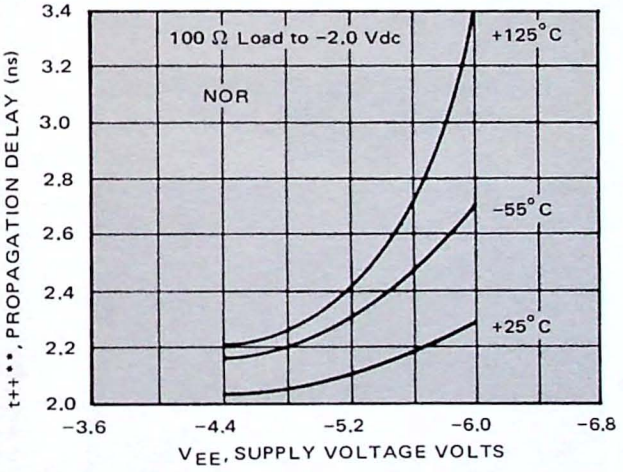
$$= -1.475\ V - (-1.600V) = 125\ mV.$$

Thus, using the worst-case design conditions, the circuits have 125 mV to guard against signal undershoot, and power or thermal disturbances. However, using typical logic levels of -0.900 volts and -1.700 volts, the circuit noise protection is greater than 200 mV for both the logic 1 and logic ∅ levels.

AC Performance

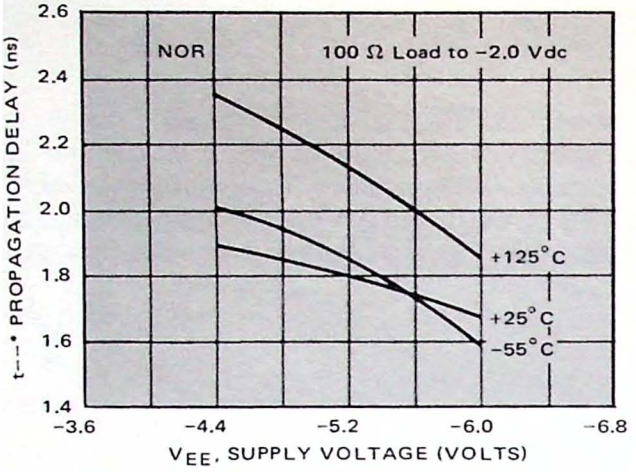
The effects of power and thermal design on noise margin were discussed in Chapters 5 and 6. The speed characteristics of MECL 10,500 and 10,600 Series parts will be affected by variations in temperature, V_{EE}, and V_{TT}. Graphs of these effects are shown in Figures 10-3 through 10-10. V_{EE} and temperature variations are shown in Figures 10-3 through 10-6; V_{TT} and temperature variations are shown in Figures 10-7 through 10-10.

10-3: Typical Propagation Delay t++ versus V_{EE} and Temperature (MC10505L)**



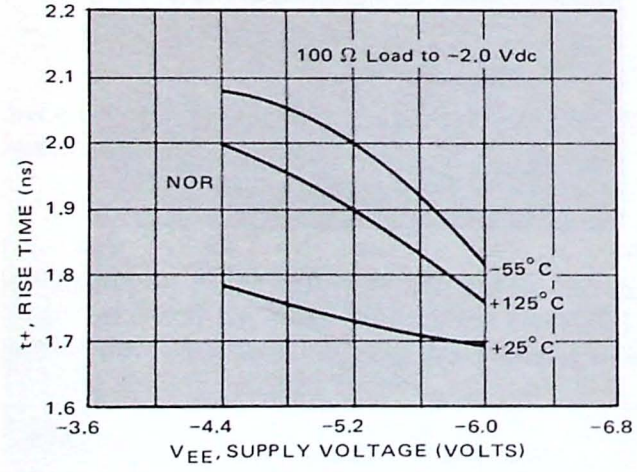
**Formerly designated t_{pd+}

10-4: Typical Propagation Delay t−−* versus V_{EE} and Temperature (MC10505L)

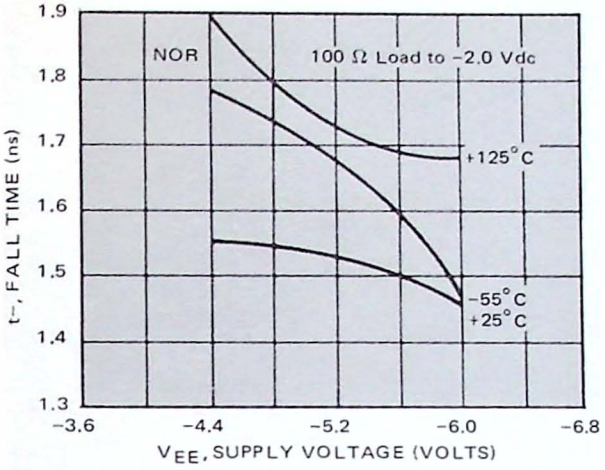


*Formerly designated $t_{pd}-$

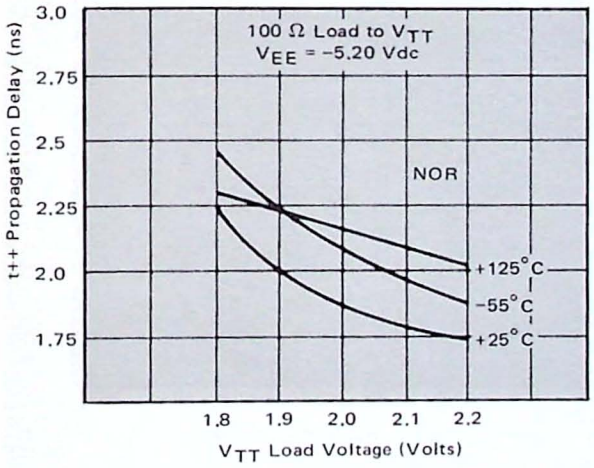
10-5: Typical Rise Time (20% to 80%) versus Temperature and Supply Voltage (MC10505L)



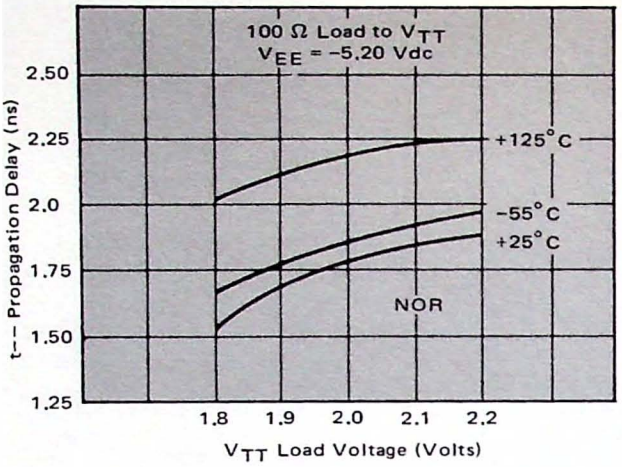
10-6: Typical Falltime
(80% to 20%) versus Temperature and V_{EE}
(MC10505L)



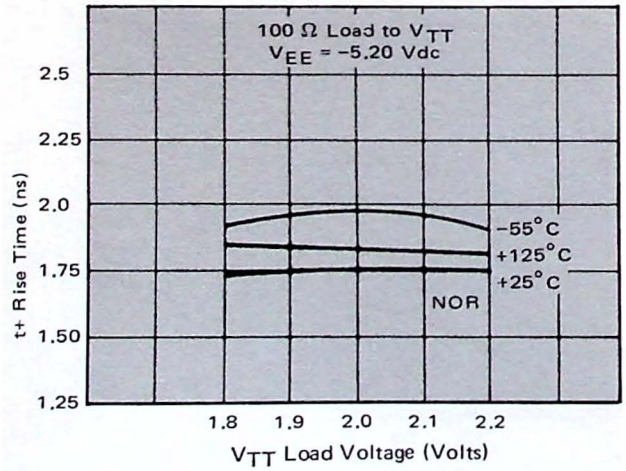
10-7: Typical Propagation Delay
t++ versus V_{TT} and Temperature
(MC10505L)



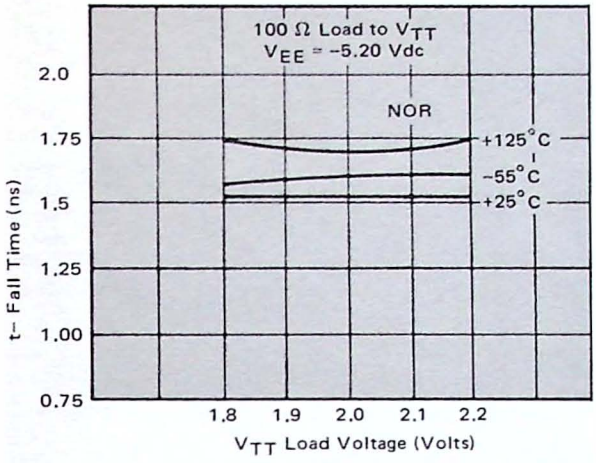
10-8: Typical Propagation Delay t−− versus V_{TT} and Temperature (MC10505L)

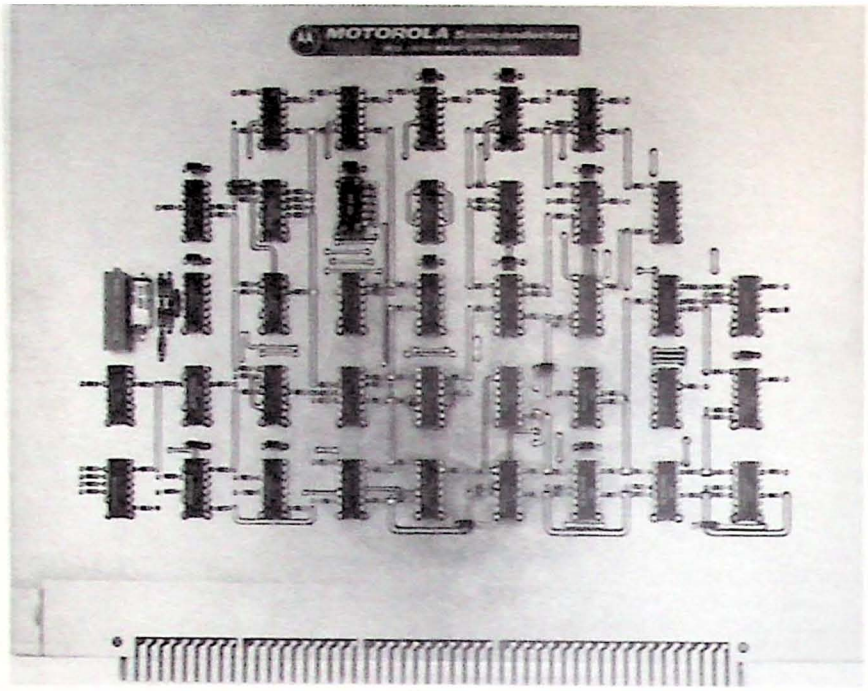


10-9: Typical Rise Time 20% to 80% t+ versus V_{TT} and Temperature (MC10505L)

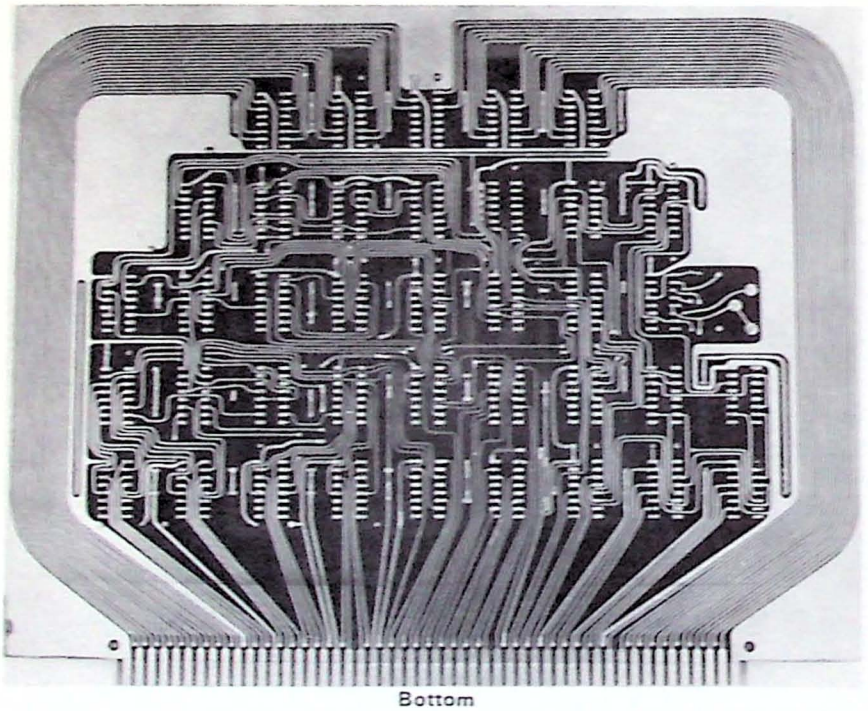


10-10: Typical Fall Time
80% to 20% t– versus V_{TT} and Temperature
(MC10505L)





Top



Bottom

MECL 10,000 logic speeds are required for controlling fast MOS memories. Shown here is the logic control circuitry for an 8k-word by 18-bit MOS memory array. On this 2-sided PC control board are 37 MECL 10,000 logic functions used for such memory requirements as timing control, refresh control, and memory/CPU interfacing. Without MECL 10,000 speeds, necessary memory control operations might take longer than a MOS memory cycle time, thus slowing memory operation. As a result, the dollar investment in a fast solid state memory might be partly wasted. With high speed MECL control logic, full memory speed can be obtained in the overall system.

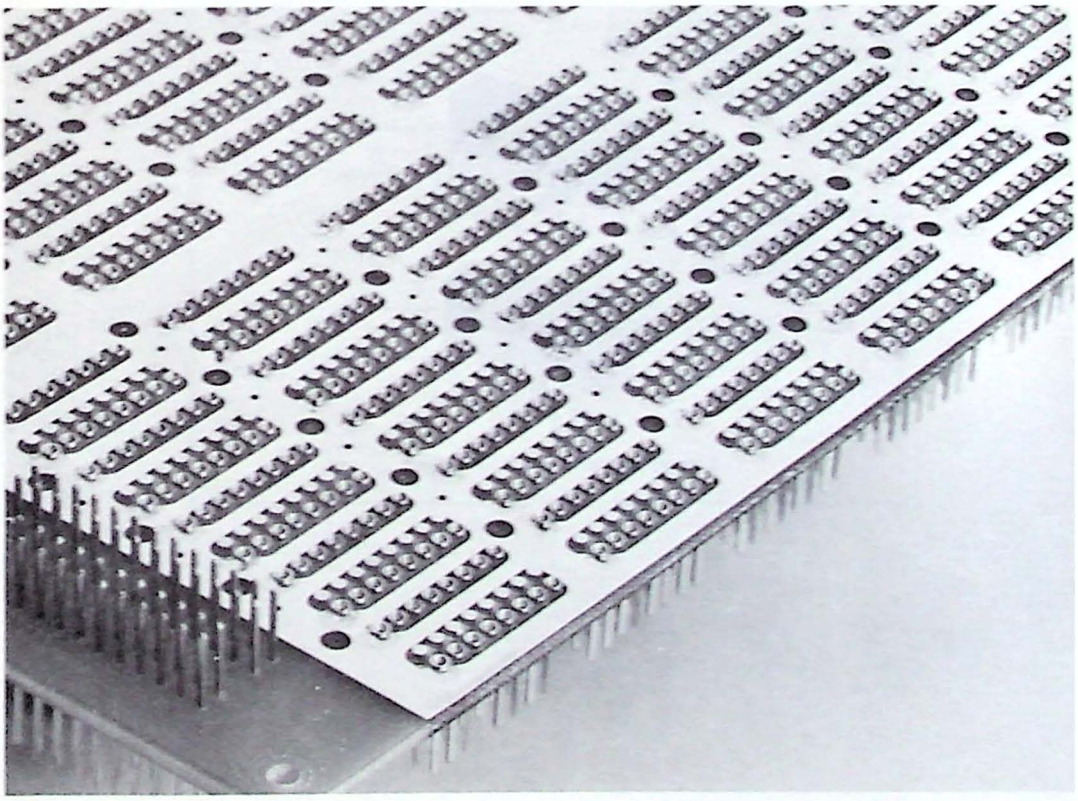
Appendix I

A successful and cost-effective logic system design is brought about by careful attention to hardware and other components, as well as by the use of the proper logic type. Some manufacturers have been developing peripheral components specifically for MECL users. Other hardware and components have appeared on the market and are proving useful in MECL systems. A few examples will be given here. No endorsement of a particular product is intended; rather, any specific components mentioned are by way of example only.

Wirewrap Boards

As mentioned in Chapter 3, wirewrap cards can be used with MECL II or MECL 10,000. At least one manufacturer (Augat Inc.) is offering boards designed specifically for use with MECL 10,000 (see Fig. 1). Boards of this type have

A-1: One type of wirewrap board designed for MECL 10,000 applications requiring high density packaging. V_{CC} plane is seen here on same side as IC package locations. V_{TT} and V_{EE} planes are on other side. Resistor tie-ins are made on the wirewrap side of the panel (bottom) to any of 4 V_{TT} pins or 4 isolated pins provided in the row between IC package pins.



planes: one for V_{CC}, one for V_{EE}, and one for V_{TT}. Provisions are included on the board for bypass capacitors, terminating or damping resistors, and flat-cable interface connections. Characteristic impedance of a wrapped line on such panels is typically 100 to 140 ohms.

Thermal Fins

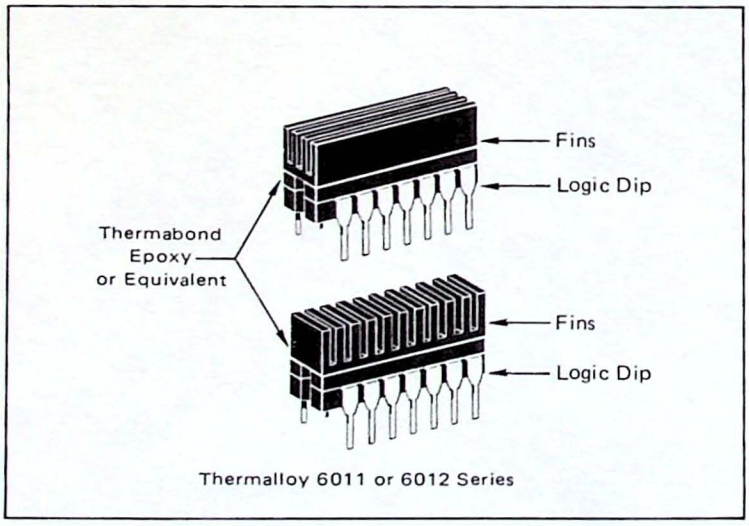
Heat sinking hardware for MECL III devices is discussed in Chapter 6. In addition, it should be pointed out that for some MECL III dual in-line packaged logic functions, finned heat dissipators, attached with thermal epoxy, may be useful. Figure 2 shows one such approach (offered by Thermalloy Co.)

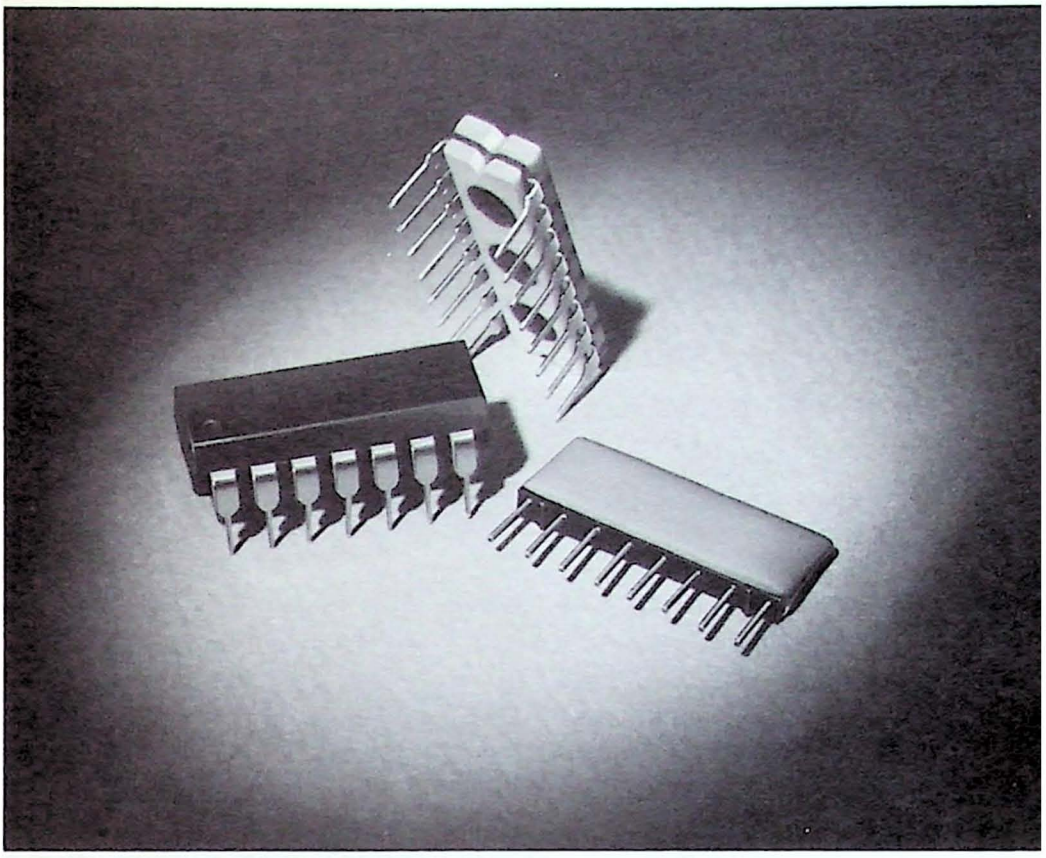
Resistor Arrays

Multiple resistors and resistor arrays are now offered by several manufacturers in dual in-line packages or in single in-line packages (see Figure 3). Either package style may be obtained with pin count, size, and spacings to mate with IC sockets. A variety of resistor values, tolerances, and power ratings are offered.

Such resistor arrays can prove useful in MECL 10,000 logic systems for uses such as series damping, gate output pulldowns, and in-line terminating with either a single resistor or a Thevenin equivalent pair.

A-2: Heat Fins useful with some MECL III logic functions.





A-3: Resistor arrays in single or dual in-line packages are available from several manufactures. Such arrays ca serve a variety of uses in system interconnections.

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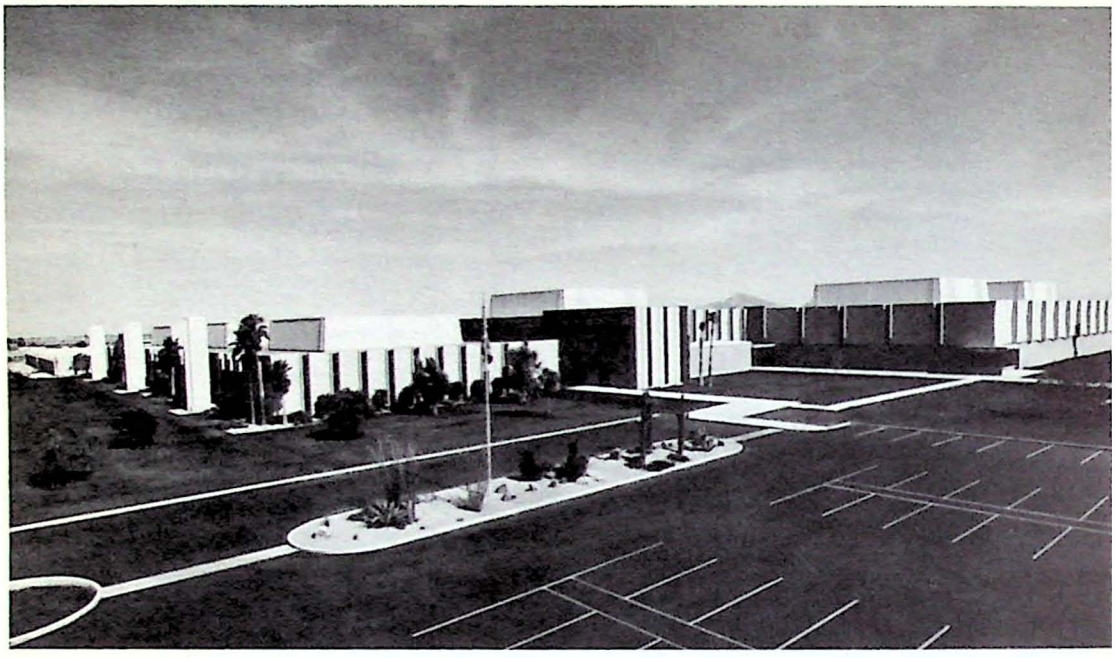

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